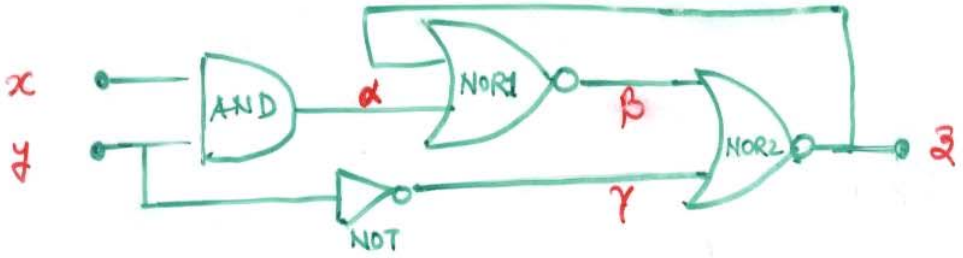
Application - Hardware Verification

- Consider the following circuit:



- When circuit is clock synchronized (inputs change with rising/falling edge of clock), and circuit is faster than clock (input-output delay less than clock period), then

$$z[n] = \overline{\overline{(x[n] \wedge y[n]) \vee z[n-1]} \vee \overline{y[n]}}$$

$$= (x[n] \vee z[n-1]) \wedge y[n]$$

So
$$\left.\begin{array}{ll} z[n-1]=0 & \Rightarrow \quad z[n] = x[n] \wedge y[n] \\ z[n-1]=1 & \Rightarrow \quad z[n] = y[n] \end{array}\right\}$$

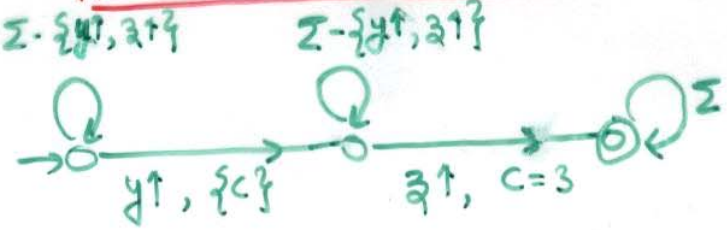
Thus $(x=1, y=0, z=0)$, $(x=1, y=1, z=1)$ are stable

- Now suppose circuit is asynchronous (inputs change randomly) and each gate has unit delay, then does this hold:

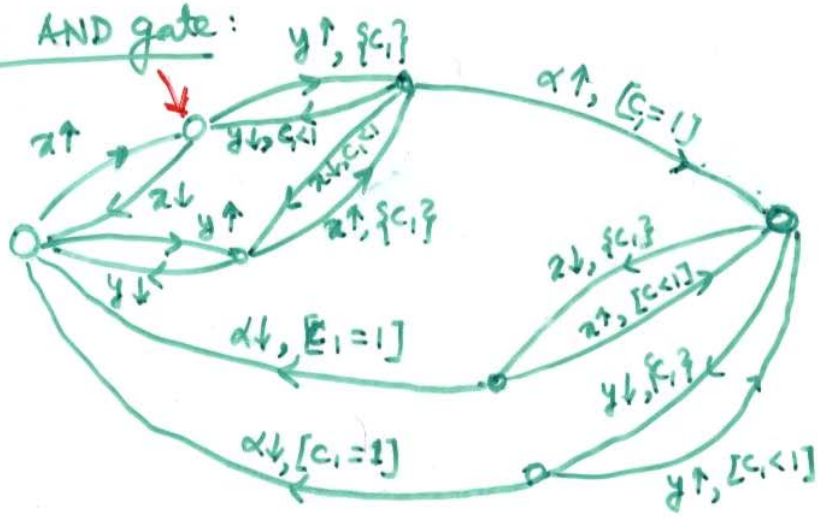
* suppose initially $(x=1, y=0, z=0)$, then z becomes high within 3 units of y becoming high?

Hardware Verification

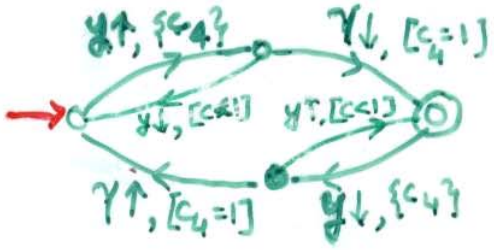
Spec:



Model of AND gate:



Model of NOT gate:



etc.

CKT = AND || NOT || NOR1 || NOR2

CKT satisfies Spec if $T_m(CKT) \subseteq T_m(spec)$

- Typically spec given as a real-time temporal logic formula
"Model checking" is used for verification. (uses data structure called BDD)