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A MULTIPATH POLYPHASE DIGITAL-TO-ANALOG CONVERTER FOR SOFTWARE RADIO TRANSMISSION SYSTEMS

D. Domanin[1], U. Gatti[2], P. Malcovati[1] and F. Maloberti[1]

[1] Integrated Microsystems Laboratory, University of Pavia
Via Ferrata 1, 27100 Pavia, Italy
Tel. +39 0382 505205, Fax. +39 0382 505677
E-Mail: domanin@ele.unipv.it, piero@ele.unipv.it, franco@ele.unipv.it

[2] Siemens ICN S. p. A., Design Center
20019 Settimo Milanese (MI), Italy
Tel. +39 02 43887415, Fax. +39 02 43888593
E-Mail: umberto.gatti@siemens-icn.it

ABSTRACT

A digital-to-analog converter system compliant with the requirements of software radio transmission interfaces is presented. The system, through a proper combination of interpolation, digital filtering and data conversion allows us to relax the speed requirements of the analog and the digital section while fully satisfying the specifications. A design example and high level simulation results are presented.

1. INTRODUCTION

Any generic telecommunication system includes two intermediate frequency (IF) and radio frequency (RF) interfaces. In the transmission path a mixer modulates the band-base signal, a power amplifier increases its power level and the result is delivered to the antenna. Nowadays more and more processing functions are implemented with digital devices (channel equalization, coding/decoding, modulation/demodulation). Then, a digital-to-analog converter (DAC) converts the result into the analog domain just before the RF interface.

A typical situation is the wide band software radio (SWR) architecture shown in Fig. 1 [1]. All the base-band channels are summed in the digital domain. The achieved wide-band signal is delivered to an high-speed high-resolution DAC and a suitable analog processing is performed before the transmission. The approach differs significantly from the one used in traditional base-band transceiver stations (BTS) which architecture is "hardware grounded". In particular a traditional solution employes a DAC per each base-band channel, thus allowing the use of DACs with rather low sampling rate and linearity. However, the analog hardware must be repeated for each channel, with an increase of volume, power consumption and costs.

Modern architectures, like the one shown in Fig. 1 and other based on the same principle, foresee the conversion from digital to analog close the antenna. The analog part is minimized and the digital section increases. Thus, we achieve a "software based" digital processing, which ensures wide-band and flexibility. In particular, for cellular mobile radio base stations they allow us to cope with different standards (Extended GSM, DCS1800, IS-95) and multiple access methods (FDMA, TDMA, CDMA).

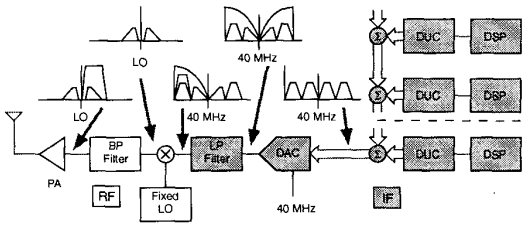

Figure 1. Block diagram of the typical software radio transmitter

The architecture shown in Fig. 1 (and others based on a similar philosophy) exhibits the two following problems:

a) Since the wide-band signal almost occupies the Nyquist interval, after the DAC it is necessary to use a complex low-pass (LP) filter to remove signal images and to equalize the "sinc" attenuation.

b) The side-band cancellation after the mixer is difficult because the modulated side bands are very close to the carrier.

This paper proposes a DAC architecture suitable to solve the two above mentioned problems. The strategy followed wants to exploit the digital processing capacities and wants to minimize the analog hardness resulting from the request of high-speed operation.

2. D/A CONVERTER ARCHITECTURE

The architecture proposed here moves from the two following observations [2]:

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1. Using a digital interpolation before the DAC relaxes the "sinc" attenuation but requires a higher conversion frequency.
2. Using a band-pass filter after an interpolator allows the low frequency and high frequency replicas of the input spectrum to be removed. Thus we can extract the optimum signal replica for relaxing either the IF and the RF filtering specifications.

These two observations lead to the architecture shown in Fig. 2. It uses an interpolation factor equal to 3 and rejects the first and the third replicas. Obviously it is possible to use an higher interpolation factor and select a more convenient replica (for example with interpolation equal to 5 we can select the third replica). However, the clock frequency either in the analog and in the digital sections increases by the interpolation factor and this can be problematic when the signal has a pretty wide band.

We can avoid the use of high speed clock in the digital part and in the data converter with the architectures shown in Fig. 3. The architecture shown in Fig. 3a achieves a clock frequency reduction in the digital section by the use of a multipath polyphase configuration. A proper design of the three transfer functions $P_0(z)$, $P_1(z)$ and $P_2(z)$ achieves the required band-pass response while using a 40 MHz clock frequency in each path. The three outputs are multiplexed to drive the DAC at 120 MHz. However, as shown in Fig. 3b it is possible to split the data conversion among the three paths and perform the multiplexing in the analog domain. If the DACs generate an output current the multiplexing is simply the current superposition. Moreover, because of the phases used, the DACs performs a return-to-zero operation as required for high resolution.

The DACs in Fig. 3b are less demanding in terms of speed than the one in Fig. 3a since, to implement the return to zero in the DAC of Fig. 3a, a switching-on period of $1 / (240\ 10^6)$ would be required, while the switching-on period of the DACs in Fig. 3b is $1 / (120\ 10^6)$. The circuit

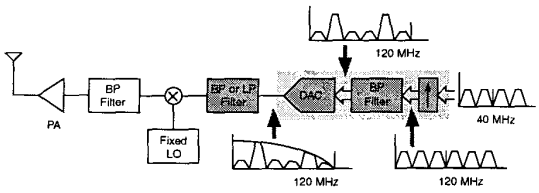

Figure 2. Block diagram of the improved software radio transmitter

shown in Fig. 3c further reduces the speed requirements. The 1 / 3 duty cycle used in Fig. 3b, indeed, becomes 1 / 2 in the architecture of Fig. 3c. Therefore, the switching-on period becomes $1 / (80\ 10^6)$. It can be observed that in the circuit of Fig. 3c the elementary time slot is $1 / (240\ 10^6)$. Therefore, we obtain an equivalent sampling frequency of 240 MHz with an actual sampling frequency of 80 MHz and 120 degrees phase shifting.

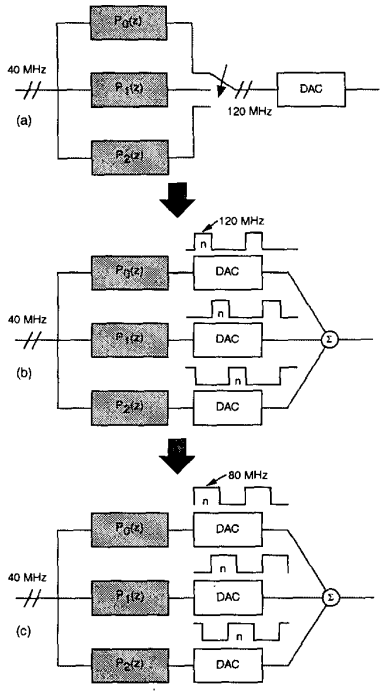

Figure 3. Block diagram of traditional polyphase filter (a), of the multipath polyphase D/A converter (b) and of the proposed architecture (c)

3. DESIGN PROCEDURE

The proposed architectures can be studied using the generic polyphase filter block diagram shown in Fig. 4. Signals

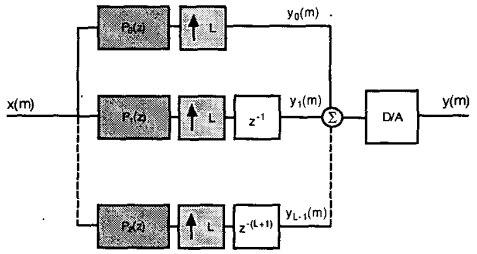

Figure 4. Equivalent circuit of the polyphase filter and DAC shown in Fig. 3a and Fig. 3b

$y_\rho(m)$, with ρ ranging from 0 to $L - 1$, represent the outputs of the polyphase filters $P_\rho(n)$. Each branch ρ in the polyphase structure provides at the output $y(m)$ samples at times $m = n\,L + \rho$. For example, the branch with $\rho = 0$ provides samples $y(0)$, $y(L)$, $y(2\,L)$ and so on. It can be shown that a structure consisting of several filters in parallel is less sensitive to parameter variations than a single stage solution, thus providing better signal-to-noise ratio [3].

The transfer function of the filter to be implemented before D/A conversion is given by

$$H(z) = \frac{N(z)}{D(z)} = \frac{\sum_{i=0}^{M} a_i z^{-i}}{1 - \sum_{j=1}^{S} b_j z^{-j}}, \quad (1)$$

where M and S denote the order of the numerator and the denominator of $H(z)$, respectively. However, in order to implement the filter with L paths in parallel, with transfer function

$$P_\rho(\zeta) = \frac{N_\rho(\zeta)}{D_\rho(\zeta)} = \frac{\sum_{i=0}^{M_\rho} C_{i,\rho}\zeta^{-i}}{1 - \sum_{j=1}^{R} E_{j,\rho}\zeta^{-j}} \quad (2)$$

and interpolation factor L ($\zeta = z^L$), $H(z)$ should be of the form

$$H(z) = \sum_{\rho=0}^{L-1} P_\rho(z^L)z^{-\rho} = \frac{\sum_{i=0}^{Q} A_i z^{-i}}{1 - \sum_{j=1}^{R} B_j z^{-jL}}, \quad (3)$$

where Q and R denote the order of the numerator and the denominator of $H(z)$, respectively. It has been shown [4] that, by using a suitable polynomial factorization, Eqn. (1) can always be rewritten as

$$H(z) = Az^{S-M}\frac{\left[\prod_{i=1}^{M}(z - z_i)\right]\left[\prod_{j=1}^{S}\left(\sum_{l=0}^{L-1} p_j^l z^{L-1-l}\right)\right]}{\prod_{k=1}^{S}(z^L - p_k^L)}, \quad (4)$$

where z_i and p_j denote the original zeroes and poles of the filter. thus obtaining a transfer function with the form specified in Eqn. (3).

Obviously, in Eqn. (4), the order of the numerator of $H(z)$ has been increased from M to $M + S(L-1)$, but the frequency response in module and phase is unchanged.

By comparing Eqn. (2) and Eqn. (3), we obtain the following rules for determining the coefficient of the L filters $P_\rho(\zeta)$:

$$\begin{cases} E_{j,\rho} = B_j, j = 1 \ldots R, \forall \rho \\ C_{k,\rho} = A_{kL+\rho}, k = 1 \ldots M_\rho, \rho = 0 \ldots L-1 \end{cases} \quad (5)$$

Fig. 5 compares in a simple case the positions of zeroes and poles of $H(z)$ from Eqn. (1) and $H(z)$ from Eqn. (3). It can

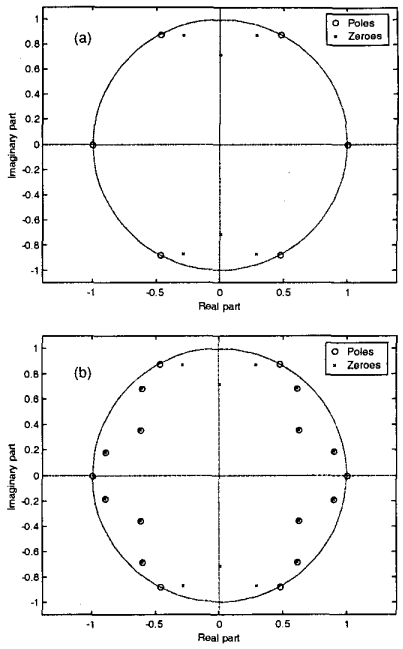

Figure 5. Example of the position of zeroes and poles of $H(z)$ from Eqn. (1) (a) and of $H(z)$ from Eqn. (3)

be observed that the extra poles introduced in Eqn. (3) are canceled by properly placed zeroes, thus maintaining the transfer function unchanged.

The previous analysis with $L = 3$ allows us to design and simulate the architectures shown in Fig. 3a and Fig. 3b. The architecture of Fig. 3c introduces an additional processing in the chain as shown in Fig. 6. Therefore the overall trans-

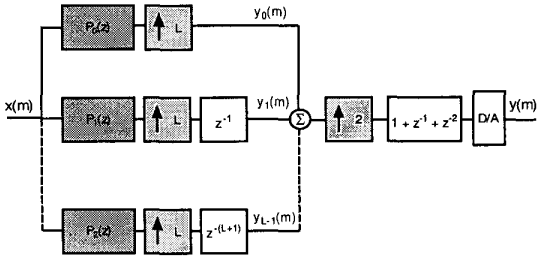

Figure 6. Equivalent circuit of the polyphase filter and DAC shown in Fig. 3c

fer function becomes

$$H'(\xi) = H(\xi^2)(1 + \xi^{-1} + \xi^{-2}), \quad (6)$$

where $\xi = \sqrt{z} = \sqrt[6]{\zeta}$.

Actually the architectures in Fig. 3b and Fig. 3c incorporate a data converter in each path. The response of the system is unchanged if the data converters used have an ideal re-

sponse. For real situations we should account for the non-idealities of the DACs. Offset and gain error mismatches are the most critical parameters. In order to estimate their effect we can shift the non-idealities through the processing chain and incorporate them in the three transfer functions P_0, P_1 and P_2. Fortunately, the reduced sensitivity to parameter variations of a multipath structure with respect to a single path solution is also effective in this case. Therefore, we expect a reduced degradation of the system response with offset and gain errors typical of modern current steering data converters.

4. DESIGN AND SIMULATION RESULTS

In order to verify the validity of the proposed technique we applied it to a practical case. A software radio architecture handles voice channels allocated in the band 5 – 15 MHz. The sampling frequency used is 40 MHz. Therefore, the margin between the used band and the Nyquist borders is 5 MHz. In order to relax the analog filter specifications it is required to interpolate by a factor 3 and attenuate the base-band and the third replica of the signal spectrum. Thus we enlarge the above mentioned margin to 25 MHz. Of course, since we use the second replica, the resulting mirroring of the spectrum has to be taken into account in the digital modulation section and in the channel allocation. For the band-pass filter we used a mask o with 80 dB of attenuation in the frequency ranges 0 – 22 MHz and 42 – 60 MHz.

We are able to meet the system specification with a 14th order band-pass filter and 14-bit coefficients. The above described design methodology allows us to design the three transfer functions P_0, P_1 and P_2 for the polyphase architecture in Fig. 3a or Fig. 3b. The achieved transfer function is shown in Fig. 7.

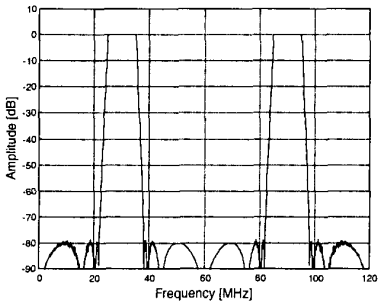

Figure 7. Simulated frequency response of the architecture shown in Fig. 3a or Fig. 3b

On the other hand, when we use the architecture shown in Fig. 3c, as already discussed, we introduce the additional filtering action defined by Eqn. (6). It can be verified that the additional term leads to a zero at 80 MHz. Fig. 8 shows the simulated frequency response. We can observe that the additional zero has two effects: it produces an attenuation of 4.5 dB in the pass-band and it attenuates by more than

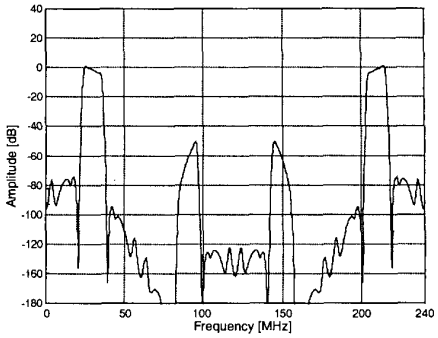

Figure 8. Simulated frequency response of the architecture shown in Fig. 3c

45 dB the spur band in the range 80 – 100 MHz. The first effect is negative and must be compensated in the digital implementation of the voice channel or by adding an emphasis in the band pass-filter. The second effect is beneficial and leads to a further relaxation of the analog filter specification.

Fig. 8 shows also the effect of offset and gain errors in the data converters. We used 12-bit DACs, with ideal response in the first path, and with +2 LSB, –2.5 LSB offset and –0.2‰, +0.14‰ gain error in the second and third path, respectively. These mismatches cause a small shift of the zero and pole positions, but the frequency response is not significantly affected. In the case of Fig. 8 the attenuation in the stop-band is worsened by only 5 dB.

5. CONCLUSIONS

In this paper we presented a digital-to-analog converter system compliant with the requirements of software radio transmission interfaces. The system, by combining interpolation, digital filtering and data conversion, allows the speed requirements and the complexity of either the analog and the digital processing to be reduced with respect to existing solutions. The validity of the proposed architecture has been verified through a design example.

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