Closed Form Solution to Simultaneous Buffer Insertion/Sizing and Wire Sizing

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In this paper, we consider the delay minimization problem of an interconnect wire by simultaneously considering buffer insertion, buffer sizing and wire sizing. We consider three cases, namely using no buffer (i.e., wire sizing alone), using a given number of buffers, and using the optimal number of buffers. We provide elegant closed form optimal solutions for all three problems. These closed form solutions are useful in early stages of the VLSI design flow such as logic synthesis and floorplanning.

Categories and Subject Descriptors: B.7.2 [**Integrated Circuits**]: Design Aids—*layout*

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1. INTRODUCTION

With the evolution of VLSI fabrication technology, interconnect delay has become the dominant factor in deep submicron design. Buffer insertion, buffer sizing, and wire sizing have been shown to be effective techniques for interconnect delay optimization. An overview of previous works on interconnect optimization using these three techniques is given in Section 2.

Although interconnect optimization is usually performed at late stages in the current VLSI design flow, it is important to take into account the impact of interconnect optimization on early stages (like high-level synthesis, logic synthesis, interconnect planning and floorplanning). However, as we can see from the overview in Section 2, except for some simple cases like wire sizing alone or buffer sizing alone, all the previous results on interconnect optimization are algorithmic. It is not practical to incorporate existing interconnect optimization

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algorithms directly into the synthesis or planning tools. Those algorithms are too costly to be run repeatedly inside the synthesis or planning tools. Moreover, to run those algorithms, a lot of detailed information (i.e., choice for wire width and buffer size) is required. But at the synthesis and planning stages, such information is usually not available. A larger degree of abstraction is usually used.

In this paper, we give closed form optimal solutions to several interconnect optimization problems. These closed form solutions are useful at the synthesis and planning stages since they are extremely efficient to compute and provide the abstraction needed.

Basically, we consider the delay minimization problem of an interconnect wire by simultaneous buffer insertion, buffer sizing, and wire sizing. The problem can be described informally as follows: Given the length of the wire, the driver resistance and load capacitance, we are allowed to divide the wire into segments and to optionally insert buffers between any two adjacent segments. The sizes of buffers and the lengths and widths of segments can all be changed in order to minimize the delay from source to sink. We solve three versions of this problem, which differ in the number buffers allowed.

The first version uses the optimal number of buffers. This version is called the simultaneous Buffer Insertion/Sizing and Wire Sizing problem (BISWS). It is defined formally as follows: The input is the wire length L, the driver resistance R_D, the load capacitance C_L (together with other electrical parameters) and the total number of segments n to be used. The output variables are listed below. Let m be the number of buffers used. (Therefore, the wire is separated by the buffers into $m + 1$ pieces.) For $0 \leq j \leq m$, let n_j be the number of segments between the jth buffer and the $(j + 1)$th buffer (with n_0 being the number of segments between the source and the first buffer and n_m being the number of segments between the last buffer and the sink). For $1 \leq j \leq m$, let b_j be the size of the jth buffer. For $1 \leq i \leq n$, let l_i and h_i be the length and the width of the ith segment, respectively. The objective is to minimize the delay D from source to sink over m, $n_0, \ldots, n_m$, $b_1, \ldots, b_m$, $l_1, \ldots, l_n$ and $h_1, \ldots, h_n$ simultaneously, with constraints $n_0 + \cdots + n_m = n$ and $l_1 + \cdots + l_n = L$. See Figure 1 for an illustration of BISWS.

The second version allows no buffer. In other words, this is the problem of delay minimization by wire sizing alone. This version is called the Wire Sizing problem (WS).

The third version is that the number of buffers m is given as input. The objective is to minimize D over $n_0, \ldots, n_m$, $b_1, \ldots, b_m$, $l_1, \ldots, l_n$ and $h_1, \ldots, h_n$ simultaneously, with constraints $n_0 + \cdots + n_m = n$ and $l_1 + \cdots + l_n = L$. This version is called the simultaneous Buffer Insertion/Sizing and Wire Sizing problem with m buffers (BISWS/m).

We provide closed form optimal solutions for all three versions. BISWS is the most sophisticated version. But we also consider WS and BISWS/m because their solutions are key intermediate steps to solve BISWS. In addition, WS and BISWS/m are also practically very interesting by themselves. Instead of using the optimal number of buffers, we may want to use fewer or not to use any at all sometimes. In those cases, we need these simpler versions.

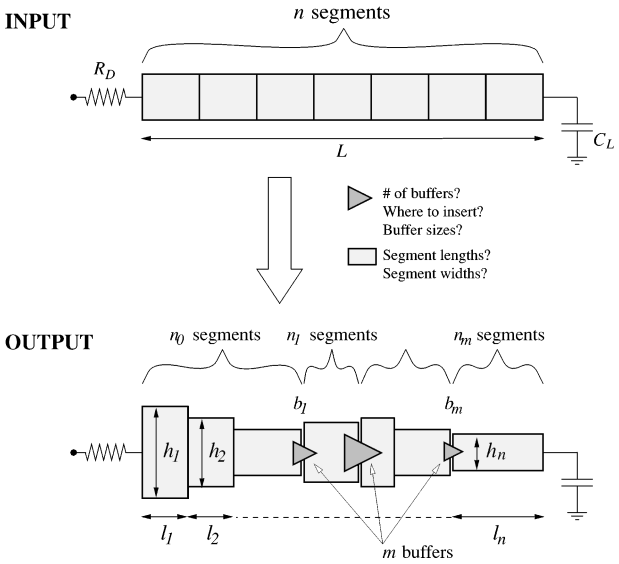

Fig. 1. Illustration of the problem BISWS. The input is L, R_D, C_L and n. The output is m, $n_0, \ldots, n_m$, $b_1, \ldots, b_m$, $l_1, \ldots, l_n$ and $h_1, \ldots, h_n$. We provide a closed form optimal solution of it which minimizes the delay.

Note that for the wire sizing technique considered here, the segment lengths can also be varied, as long as the total length is fixed. This is more general than the formulations in previous works, which allow the change of segment widths only. The buffer insertion technique is more general too as buffers can be inserted anywhere, rather than having some predefined candidate buffer locations [Alpert and Devgan 1997; Lillis et al. 1995]. On the other hand, bounds on buffer size and wire width, and wire fringing capacitance are ignored in the problem formulation. The consideration of these two extensions are presented in Section 7.4 and 7.5, respectively. Also note that n is a parameter that allows us to determine the quality of the solution. We can get a smaller delay by using a larger value of n.

The remainder of this paper is organized as follows: In Section 2, we present an overview of previous works on interconnect optimization. In Section 3, we introduce some notations and the models that we use. In Section 4, we consider WS. The closed form solution is summarized in Theorem 1. In Section 5, we consider BISWS/m. The closed form solution is summarized in Theorem 2. Then, in Section 6, by showing how to find the optimal number of buffers, we give a closed form solution for BISWS. The result is summarized in Theorem 3. In Section 7, we present some interesting implications and extensions of our closed form solutions. An extended abstract of this paper was presented in ISPD-97 [Chu and Wong 1997].

2. PREVIOUS WORKS

In this section, an overview of previous works on interconnect optimization using buffer insertion, buffer sizing and wire sizing is presented.

For wire sizing, Chen et al. [1996b], and Fishburn and Schevon [1995] gave a closed form solution to the continuous wire sizing problem. Later, Chen and Wong [1997], Fishburn [1997], and Gao and Wong [1997] extended the result by taking fringing capacitance into consideration. Many iterative algorithms optimizing various objectives using different delay models have also been proposed Chen and Wong [1996]; Cong and He [1996]; Cong and Leung [1993]; Kay et al. [1997]; Menezes et al. [1997]; Menezes et al. [1994]; Xue et al. [1996].

Buffer sizing has been an active research area for decades. To drive a large capacitive load, Lin and Linholm [1975] first proposed the tapered buffer structure, which is a series of cascaded buffers of increasing size. Immediately after that, Jaeger [1975] showed that the optimal tapering factor (the size-ratio between consecutive buffers in the tapered buffer structure) that minimizes delay should be the constant e. Hedenstierna and Jeppson [1987] considered a more accurate capacitance model and delay model, and showed that the optimal tapering factor should be approximately 3–5, depending on the process parameters and the design style. Zhou and Liu [1997] considered delay, power dissipation and circuit area and proposed the use of variable size-ratio between consecutive buffers. Note that all the results for the tapered buffer structure above are useful only when large capacitive loads are driven. When the resistiveness of loads cannot be ignored, as in the case of driving interconnects nowadays, buffers should be distributed throughout the interconnect.

If the buffer locations in an interconnect are predetermined, and the buffers and wire segments can be sized simultaneously, many iterative algorithms using various techniques have been published in the past few years. Menezes et al. [1995] used a sequential quadratic programming approach, Cong et al. [1996] used a greedy approach, Chen et al. [1996a] used the Lagrangian relaxation technique, and Chu and Wong [1999b] solved a recurrence relation.

If the buffer locations are not predetermined (i.e., buffer insertion is considered), Dhar and Franklin [1991], and Alpert and Devgan [1997] considered the problem of driving a uniform line (i.e., wires were not sized). Dhar and Franklin [1991] assumed that the driver and sink can be resized and derived a closed form solution which minimizes the delay. Alpert and Devgan [1997] disallowed resizing of driver and sink and obtained a theoretical result similar to Dhar and Franklin [1991]. Chu and Wong [1999a] formulated the simultaneous buffer insertion and wire sizing problem as a convex quadratic program and derived an very efficient algorithm to solve it. They also introduced an effective pruning technique to handle buffer sizing. Lillis, et al. [1995] handled the simultaneous buffer insertion, buffer sizing and wire sizing problem by generalizing the dynamic programming algorithm for buffer insertion in van Ginneken [1990]. The algorithm in Lillis et al. [1995] was later extended to handle power dissipation and incorporate signal slew into the buffer delay model Lillis et al. [1996].

As we can see, except for some simple cases like wire sizing alone or buffer sizing alone, all the previous results on interconnect optimization are algorithmic.

3. PRELIMINARIES

The following are the notations of the electrical parameters used in this paper:

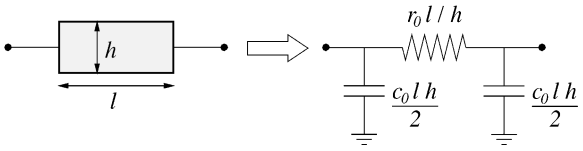

Fig. 2. The model of a wire segment of length l and width h by a π-type RC circuit.

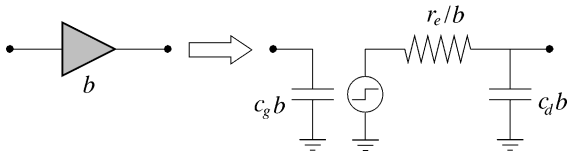

Fig. 3. The model of a buffer of size $b \times$ minimum device by a switch-level RC circuit.

- R_D: Driver resistance.
- C_L: Load capacitance.
- r_0: Unit square wire resistance.
- c_0: Unit area wire capacitance.
- r_e: Effective output resistance of a minimum device.
- c_g: Gate capacitance of a minimum device.
- c_d: Drain capacitance of a minimum device.

Elmore delay model [Elmore, 1948] is used for delay calculation. For the purpose of delay calculation, a wire segment is modeled as a π-type RC circuit as shown in Figure 2, and a buffer is modeled as a switch-level RC circuit as shown in Figure 3. For any segment, the *upstream resistance* is the sum of all resistances from the driver (or the last buffer before the segment) to the segment (excluding the segment). The *downstream capacitance* is the sum of all capacitances from the segment (excluding the segment) to the sink (or the next buffer after the segment). The upstream resistance of a buffer or the load, and the downstream capacitance of a buffer or the driver are defined similarly. Let the delay associated with the driver be $R_D \times$ (downstream capacitance of the driver), the delay associated with a wire segment as shown in Figure 2 be $(r_0 l/h) \times (c_0 l h/2 +$ downstream capacitance of the segment), and the delay associated with a buffer as shown in Figure 3 be $(r_e/b) \times (c_d b +$ downstream capacitance of the buffer). Then, the Elmore delay for the wire is the sum of the delays associated with the driver, all the segments and all the buffers.

4. WIRE SIZING

In this section, we consider the case when no buffer is used. In other words, we consider the delay minimization problem from source to sink by sizing the n segments of the wire. We call this the Wire Sizing problem (WS). See Figure 4 for an illustration.

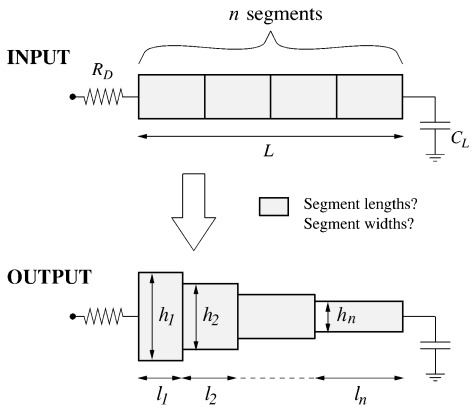

Fig. 4. Illustration of the problem WS. The input is L, R_D, C_L and n. The output is $l_1, \ldots, l_n$ and $h_1, \ldots, h_n$. We provide a closed form optimal solution of it which minimizes the delay.

The delay D can be written as a function of l_i's and h_i's, as follows:

$$\begin{aligned} D \;=\; & R_D(c_0 l_1 h_1 + c_0 l_2 h_2 + \cdots + c_0 l_n h_n + C_L) \\ & + \frac{r_0 l_1}{h_1}\left(\frac{c_0 l_1 h_1}{2} + c_0 l_2 h_2 + \cdots + c_0 l_n h_n + C_L\right) \\ & + \frac{r_0 l_2}{h_2}\left(\frac{c_0 l_2 h_2}{2} + \cdots + c_0 l_n h_n + C_L\right) \\ & \quad \vdots \\ & + \frac{r_0 l_n}{h_n}\left(\frac{c_0 l_n h_n}{2} + C_L\right). \end{aligned}$$

We want to minimize D with respect to l_i's and h_i's. The optimal l_i's is given in Lemma 5, and the optimal h_i's is given in Lemma 7. The optimal solution of WS is summarized in Theorem 1. In particular, it is interesting to note that for the optimal solution, the wire is divided into equal-length segments and the widths of the segments form a geometric progression (i.e., for $1 \le i \le n$, $h_i = h_1 \alpha^{i-1}$ for some constant h_1 and α).

LEMMA 1. *If $f(x) = Ax + B/x + C$ where A, B, C are independent of x, and $A > 0$, $B > 0$, then $f(x)$ is minimized when $x = \sqrt{B/A}$.*

PROOF. x is an extreme point when $f'(x) = A - B/x^2 = 0$. Therefore $x = \sqrt{B/A}$. $f''(\sqrt{B/A}) = 2B/(\sqrt{B/A})^3 = 2A\sqrt{A/B} > 0$. So $f(x)$ is minimized when $x = \sqrt{B/A}$. □

LEMMA 2. *If $f(x) = Ax^2 + Bx + C$ where A, B, C are independent of x and $A > 0$, then $f(x)$ is minimized when $x = -B/(2A)$.*

PROOF. x is an extreme point when $f'(x) = 2Ax + B = 0$. Therefore, $x = -B/(2A)$. $f''(x) = 2A > 0$. So $f(x)$ is minimized when $x = -B/(2A)$. □

LEMMA 3. *For the optimal solution of WS, for any i such that $1 \le i \le n$, $h_i = \sqrt{r_0 C_{\mathcal{D}} / c_0 R_{\mathcal{U}}}$, and $D = r_0 c_0 l_i^2/2 + 2 l_i \sqrt{r_0 c_0 R_{\mathcal{U}} C_{\mathcal{D}}} + R_{\mathcal{U}} C_{\mathcal{D}} +$ (terms independent of h_i), where $R_{\mathcal{U}}$ is the upstream resistance and $C_{\mathcal{D}}$ is the downstream capacitance of segment i.*

PROOF. The delay D can be written in terms of h_i as follows:

$$\begin{aligned} D &= R_{\mathcal{U}}(c_0 l_i h_i + C_{\mathcal{D}}) + \frac{r_0 l_i}{h_i}\left(\frac{c_0 l_i h_i}{2} + C_{\mathcal{D}}\right) \\ &\quad + \text{terms independent of } h_i \\ &= h_i \cdot R_{\mathcal{U}} c_0 l_i + \frac{1}{h_i} \cdot r_0 C_{\mathcal{D}} l_i + \frac{r_0 c_0 l_i^2}{2} + R_{\mathcal{U}} C_{\mathcal{D}} \\ &\quad + \text{terms independent of } h_i. \end{aligned}$$

By Lemma 1, optimal

$$h_i = \sqrt{\frac{r_0 C_{\mathcal{D}} l_i}{R_{\mathcal{U}} c_0 l_i}} = \sqrt{\frac{r_0 C_{\mathcal{D}}}{c_0 R_{\mathcal{U}}}}.$$

If we substitute h_i into D,

$$D = \frac{r_0 c_0 l_i^2}{2} + 2 l_i \sqrt{r_0 c_0 R_{\mathcal{U}} C_{\mathcal{D}}} + R_{\mathcal{U}} C_{\mathcal{D}} + \text{terms independent of } h_i. \quad \square$$

LEMMA 4. *For the optimal solution of WS, $h_1 > h_2 > \cdots > h_n$.*

PROOF. Consider segment i and segment $i+1$ for any i, the upstream resistance of segment i is smaller than that of segment $i+1$ and the downstream capacitance of segment i is larger than that of segment $i+1$. So by Lemma 3, $h_i > h_{i+1}$ for the optimal solution. $\square$

LEMMA 5. *For the optimal solution of WS, $l_1 = l_2 = \cdots = l_n = L/n$.*

PROOF. Consider segment i and segment $i+1$. Let $\hat{L} = l_i + l_{i+1}$. We assume in this proof that $\hat{L}$ is fixed while l_i and l_{i+1} are considered as variables, and h_i and h_{i+1} are changed optimally according to l_i and l_{i+1}. We show below that the delay is minimized when $l_i = l_{i+1}$. It follows that, for any solution of WS, if $l_i \neq l_{i+1}$ for some i, we can always find a better solution with $l_i = l_{i+1}$. Therefore, for the optimal solution, all l_i's must be the same.

Let $R_{\mathcal{U}}$ be the upstream resistance of segment i and $C_{\mathcal{D}}$ be the downstream capacitance of segment $i+1$. Note that $R_{\mathcal{U}}$ and $C_{\mathcal{D}}$ are independent of h_i, h_{i+1}, l_i and l_{i+1} as $l_i + l_{i+1}$ is fixed.

$$\begin{aligned} D &= R_{\mathcal{U}}(c_0 l_i h_i + c_0 l_{i+1} h_{i+1} + C_{\mathcal{D}}) + \frac{r_0 l_i}{h_i}\left(\frac{c_0 l_i h_i}{2} + c_0 l_{i+1} h_{i+1} + C_{\mathcal{D}}\right) \\ &\quad + \frac{r_0 l_{i+1}}{h_{i+1}}\left(\frac{c_0 l_{i+1} h_{i+1}}{2} + C_{\mathcal{D}}\right) \\ &\quad + \text{terms independent of } h_i, h_{i+1}, l_i \text{ and } l_{i+1} \end{aligned}$$

$$= \left(r_0c_0 - \frac{r_0c_0h_{i+1}}{h_i}\right)l_i^2 + \left(R_{\mathcal{U}}c_0h_i - R_{\mathcal{U}}c_0h_{i+1} + \frac{r_0c_0h_{i+1}\hat{L}}{h_i} + \frac{r_0C_{\mathcal{D}}}{h_i} - r_0c_0\hat{L} - \frac{r_0C_{\mathcal{D}}}{h_{i+1}}\right)l_i + \text{terms independent of } h_i, h_{i+1}, l_i \text{ and } l_{i+1}.$$

By Lemma 4, $r_0c_0 - r_0c_0h_{i+1}/h_i > 0$. So by Lemma 2,

$$l_i = \frac{-(R_{\mathcal{U}}c_0h_i - R_{\mathcal{U}}c_0h_{i+1} + r_0c_0h_{i+1}\hat{L}/h_i + r_0C_{\mathcal{D}}/h_i - r_0c_0\hat{L} - r_0C_{\mathcal{D}}/h_{i+1})}{2(r_0c_0 - r_0c_0h_{i+1}/h_i)}$$

$$= \frac{1}{2}\left(\hat{L} + \frac{C_{\mathcal{D}}}{c_0}\frac{1}{h_{i+1}} - \frac{R_{\mathcal{U}}}{r_0}h_i\right). \quad (1)$$

By Lemma 3,

$$h_i = \sqrt{\frac{r_0(c_0l_{i+1}h_{i+1} + C_{\mathcal{D}})}{c_0R_{\mathcal{U}}}}.$$

So

$$l_{i+1} = \frac{R_{\mathcal{U}}}{r_0}\frac{{h_i}^2}{h_{i+1}} - \frac{C_{\mathcal{D}}}{c_0}\frac{1}{h_{i+1}}. \quad (2)$$

Again, by Lemma 3,

$$h_{i+1} = \sqrt{\frac{r_0C_{\mathcal{D}}}{c_0(R_{\mathcal{U}} + r_0l_i/h_i)}}.$$

So

$$l_i = \frac{C_{\mathcal{D}}}{c_0}\frac{h_i}{h_{i+1}^2} - \frac{R_{\mathcal{U}}}{r_0}h_i. \quad (3)$$

Add (2) and (3),

$$\hat{L} = \frac{R_{\mathcal{U}}}{r_0}\frac{h_i^2}{h_{i+1}} - \frac{C_{\mathcal{D}}}{c_0}\frac{1}{h_{i+1}} + \frac{C_{\mathcal{D}}}{c_0}\frac{h_i}{h_{i+1}^2} - \frac{R_{\mathcal{U}}}{r_0}h_i. \quad (4)$$

Eliminate l_i by (1) and (3),

$$\frac{1}{2}\hat{L} = \frac{C_{\mathcal{D}}}{c_0}\frac{h_i}{h_{i+1}^2} - \frac{1}{2}\frac{R_{\mathcal{U}}}{r_0}h_i - \frac{1}{2}\frac{C_{\mathcal{D}}}{c_0}\frac{1}{h_{i+1}}. \quad (5)$$

Subtract $2 \times (5)$ from (4),

$$\frac{C_{\mathcal{D}}}{c_0}\frac{h_i}{h_{i+1}^2} = \frac{R_{\mathcal{U}}}{r_0}\frac{h_i^2}{h_{i+1}},$$

which implies

$$\frac{C_{\mathcal{D}}}{c_0}\frac{1}{h_{i+1}} = \frac{R_{\mathcal{U}}}{r_0}h_i.$$

So by (1), $l_i = \hat{L}/2$. That means $l_i = l_{i+1} = \hat{L}/2$. This implies $l_1 = l_2 = \cdots = l_n = L/n$ for the optimal solution. □

LEMMA 6. *For the optimal solution of WS, $h_1, h_2, \ldots, h_n$ form a geometric progression.*

PROOF. Consider segment i, segment $i+1$ and segment $i+2$. Let $R_{\mathcal{U}}$ be the upstream resistance of segment i and $C_{\mathcal{D}}$ be the downstream capacitance of segment $i+2$. Let $l = L/n$. By Lemma 5, $l_i = l_{i+1} = l_{i+2} = l$. Let $R = R_{\mathcal{U}}/r_0 l$ and $C = C_{\mathcal{D}}/c_0 l$. By Lemma 3,

$$\begin{aligned} h_i &= \sqrt{\frac{r_0(c_0 l h_{i+1} + c_0 l h_{i+2} + C_{\mathcal{D}})}{c_0 R_{\mathcal{U}}}} \\ &= \sqrt{\frac{h_{i+1} + h_{i+2} + C}{R}}, \qquad (6) \\ h_{i+1} &= \sqrt{\frac{r_0(c_0 l h_{i+2} + C_{\mathcal{D}})}{c_0(R_{\mathcal{U}} + r_0 l/h_i)}} \\ &= \sqrt{\frac{h_{i+2} + C}{1/h_i + R}}, \qquad (7) \\ h_{i+2} &= \sqrt{\frac{r_0 C_{\mathcal{D}}}{c_0(R_{\mathcal{U}} + r_0 l/h_i + r_0 l/h_{i+1})}} \\ &= \sqrt{\frac{C}{1/h_i + 1/h_{i+1} + R}}. \qquad (8) \end{aligned}$$

So by (6), (7), and (8), respectively,

$$h_i^2 R = h_{i+1} + h_{i+2} + C \qquad (9)$$

$$\frac{h_{i+1}^2}{h_i} + h_{i+1}^2 R = h_{i+2} + C \qquad (10)$$

$$\frac{h_{i+2}^2}{h_i} + \frac{h_{i+2}^2}{h_{i+1}} + h_{i+2}^2 R = C. \qquad (11)$$

Eliminate C by (9) and (11),

$$h_i^2 R = h_{i+1} + h_{i+2} + \frac{h_{i+2}^2}{h_i} + \frac{h_{i+2}^2}{h_{i+1}} + h_{i+2}^2 R. \qquad (12)$$

Eliminate $h_{i+2} + C$ by (9) and (10),

$$h_i^2 R = h_{i+1} + \frac{h_{i+1}^2}{h_i} + h_{i+1}^2 R. \qquad (13)$$

Eliminate R by (12) and (13),

$$\begin{aligned} &(h_i^2 - h_{i+1}^2)\left(h_{i+1} + h_{i+2} + \frac{h_{i+2}^2}{h_i} + \frac{h_{i+2}^2}{h_{i+1}}\right) \\ &= (h_i^2 - h_{i+2}^2)\left(h_{i+1} + \frac{h_{i+1}^2}{h_i}\right) \end{aligned}$$

$$\Leftrightarrow \frac{h_i^2}{h_{i+1}^2}\frac{h_{i+2}}{h_{i+1}} + \frac{h_i}{h_{i+1}}\frac{h_{i+2}^2}{h_{i+1}^2} + \frac{h_i^2}{h_{i+1}^2}\frac{h_{i+2}^2}{h_{i+1}^2} - 1 - \frac{h_{i+2}}{h_{i+1}} - \frac{h_i}{h_{i+1}} = 0$$
$$\Leftrightarrow \left(\frac{h_i}{h_{i+1}}\frac{h_{i+2}}{h_{i+1}} - 1\right)\left(\frac{h_i}{h_{i+1}} + 1\right)\left(\frac{h_{i+2}}{h_{i+1}} + 1\right) = 0$$
$$\Leftrightarrow \frac{h_i}{h_{i+1}}\frac{h_{i+2}}{h_{i+1}} - 1 = 0 \quad \text{as } \frac{h_i}{h_{i+1}} + 1 > 0 \qquad \text{and} \qquad \frac{h_{i+2}}{h_{i+1}} + 1 > 0$$
$$\Leftrightarrow \frac{h_{i+1}}{h_i} = \frac{h_{i+2}}{h_{i+1}}.$$

So h_i's form a geometric progression. □

LEMMA 7. *For the optimal solution of WS, we have*

$$h_i = \sqrt{\frac{r_0 C_L}{c_0 R_D}\frac{1}{\alpha^{n-1}}}\alpha^{i-1} \qquad \textit{for} \quad 1 \le i \le n$$
$$D = \frac{r_0 c_0 L^2}{2n^2} \cdot \frac{n + 2\alpha - n\alpha^2}{(1-\alpha)^2},$$

where α is the unique root between 0 and 1 of

$$f(\alpha) = \frac{L}{n}\sqrt{\frac{r_0 c_0}{R_D C_L}}\alpha^{(n+1)/2} + \alpha - 1.$$

PROOF. Let $l = L/n$. By Lemma 5, $l_i = l$ for $1 \le i \le n$. By Lemma 6, we know $h_i = h_1\alpha^{i-1}$, $1 \le i \le n$, for some α. By Lemma 4, we know $0 < \alpha < 1$. We can write the delay as

$$\begin{aligned} D &= R_D\left(c_0 l h_1 + c_0 l h_1\alpha + \cdots + c_0 l h_1\alpha^{n-1} + C_L\right) \\ &\quad + \frac{r_0 l}{h_1}\left(\frac{c_0 l h_1}{2} + c_0 l h_1\alpha + \cdots + c_0 l h_1\alpha^{n-1} + C_L\right) \\ &\quad + \frac{r_0 l}{h_1\alpha}\left(\frac{c_0 l h_1\alpha}{2} + \cdots + c_0 l h_1\alpha^{n-1} + C_L\right) \\ &\quad \vdots \\ &\quad + \frac{r_0 l}{h_1\alpha^{n-1}}\left(\frac{c_0 l h_1\alpha^{n-1}}{2} + C_L\right) \\ &= R_D C_L + r_0 c_0 l^2\frac{n}{2} + r_0 c_0 l^2((n-1)\alpha + (n-2)\alpha^2 + \cdots + 2\alpha^{n-2} + \alpha^{n-1}) \\ &\quad + R_D c_0 l h_1(1 + \alpha + \cdots + \alpha^{n-1}) + \frac{r_0 l C_L}{h_1}\left(1 + \frac{1}{\alpha} + \cdots + \frac{1}{\alpha^{n-1}}\right). \end{aligned} \tag{14}$$

View D as a function of h_1 and apply Lemma 1, we get

$$\begin{aligned} h_1 &= \sqrt{\frac{r_0 l C_L(1 + 1/\alpha + \cdots + 1/\alpha^{n-1})}{R_D c_0 l(1 + \alpha + \cdots + \alpha^{n-1})}} \\ &= \sqrt{\frac{r_0 C_L(1 + \alpha + \cdots + \alpha^{n-1})/\alpha^{n-1}}{c_0 R_D(1 + \alpha + \cdots + \alpha^{n-1})}} = \sqrt{\frac{r_0 C_L}{c_0 R_D}\frac{1}{\alpha^{n-1}}}. \end{aligned}$$

Substitute h_1 into (14), we get

$$\begin{aligned}
D &= R_D C_L + r_0 c_0 l^2 \frac{n}{2} + r_0 c_0 l^2((n-1)\alpha + (n-2)\alpha^2 + \cdots + 2\alpha^{n-2} + \alpha^{n-1}) \\
&\quad + R_D c_0 l \sqrt{\frac{r_0 C_L}{c_0 R_D} \frac{1}{\alpha^{n-1}}}(1 + \alpha + \cdots + \alpha^{n-1}) \\
&\quad + r_0 l C_L \sqrt{\frac{c_0 R_D}{r_0 C_L} \alpha^{n-1}} \left(1 + \frac{1}{\alpha} + \cdots + \frac{1}{\alpha^{n-1}}\right) \\
&= R_D C_L + r_0 c_0 l^2 \frac{n}{2} + r_0 c_0 l^2((n-1)\alpha + (n-2)\alpha^2 + \cdots + 2\alpha^{n-2} + \alpha^{n-1}) \\
&\quad + 2l\sqrt{r_0 c_0 R_D C_L}\left(\alpha^{-(n-1)/2} + \alpha^{-(n-3)/2} + \cdots + \alpha^{(n-1)/2}\right) \qquad (15) \\
&= R_D C_L + r_0 c_0 l^2 \frac{n}{2} + r_0 c_0 l^2 \left(\frac{\alpha^{n+1} - n\alpha^2 + (n-1)\alpha}{(1-\alpha)^2}\right) \\
&\quad + 2l\sqrt{r_0 c_0 R_D C_L}\left(\frac{1}{\alpha^{(n-1)/2}} \cdot \frac{1-\alpha^n}{1-\alpha}\right). \qquad (16)
\end{aligned}$$

Let $\sigma = \sqrt{r_0 c_0 R_D C_L}$.

$$\begin{aligned}
\frac{dD}{d\alpha} &= r_0 c_0 l^2 \left(\frac{(n+1)\alpha^n - 2n\alpha + (n-1)}{(1-\alpha)^2} + \frac{2(\alpha^{n+1} - n\alpha + (n-1)\alpha)}{(1-\alpha)^3}\right) \\
&\quad + 2l\sigma \left(\frac{1}{\alpha^{\frac{n-1}{2}}} \frac{1}{1-\alpha}(-n\alpha^{n-1}) + \frac{1-\alpha^n}{1-\alpha}\left(-\frac{n-1}{2}\right)\frac{1}{\alpha^{(n+1)/2}}\right. \\
&\qquad \left. + \frac{1-\alpha^n}{\alpha^{\frac{n-1}{2}}} \frac{1}{(1-\alpha)^2}\right) \\
&= r_0 c_0 l^2 \frac{(n-1) - (n+1)\alpha + (n+1)\alpha^n - (n-1)\alpha^{n+1}}{(1-\alpha)^3} \\
&\quad - l\sigma \frac{(n-1) - (n+1)\alpha + (n+1)\alpha^n - (n-1)\alpha^{n+1}}{\alpha^{(n+1)/2}(1-\alpha)^2} \\
&= \left(\frac{r_0 c_0 l}{1-\alpha} - \frac{\sigma}{\alpha^{(n+1)/2}}\right) \frac{l}{(1-\alpha)^2}((n-1) - (n+1)\alpha + (n+1)\alpha^n - (n-1)\alpha^{n+1}).
\end{aligned}$$

Note that $l \neq 0$ and $(1-\alpha)^2 \neq 0$ as $0 < \alpha < 1$. Let

$$p(\alpha) = (n-1) - (n+1)\alpha + (n+1)\alpha^n - (n-1)\alpha^{n+1}.$$

Then

$$\begin{aligned}
p'(\alpha) &= -(n+1) + n(n+1)\alpha^{n-1} - (n-1)(n+1)\alpha^n \\
p''(\alpha) &= n(n-1)(n+1)\alpha^{n-2} - n(n-1)(n+1)\alpha^{n-1} \\
&= n(n-1)(n+1)\alpha^{n-2}(1-\alpha) \\
&> 0 \qquad \text{for} \quad 0 < \alpha < 1.
\end{aligned}$$

So $p'(\alpha)$ is increasing for $0 < \alpha < 1$. As $p'(1) = 0$, $p'(\alpha) < 0$ for $0 < \alpha < 1$. Hence, $p(\alpha)$ is decreasing for $0 < \alpha < 1$. As $p(1) = 0$, $p(\alpha) > 0$ for $0 < \alpha < 1$. In other words, $p(\alpha) \neq 0$ as $0 < \alpha < 1$.

By (15), D is a posynomial [Duffin et al. 1967] in α. So D has a unique minimum with respect to α. Therefore

$$\begin{aligned} D \text{ is minimized} &\Leftrightarrow \frac{dD}{d\alpha} = 0 \\ &\Leftrightarrow \left(\frac{r_0 c_0 l}{1-\alpha} - \frac{\sigma}{\alpha^{(n+1)/2}} \right) = 0 \\ &\Leftrightarrow l\sqrt{\frac{r_0 c_0}{R_D C_L}}\alpha^{(n+1)/2} + \alpha - 1 = 0. \end{aligned}$$

Let

$$f(\alpha) = \frac{L}{n}\sqrt{\frac{r_0 c_0}{R_D C_L}}\alpha^{(n+1)/2} + \alpha - 1.$$

Then the optimal value of α which minimizes D is a root of $f(\alpha)$ between 0 and 1. Note that

$$f(0) < 0 < f(1)$$

and

$$f'(\alpha) = \frac{L}{n}\sqrt{\frac{r_0 c_0}{R_D C_L}} \cdot \frac{n+1}{2}\alpha^{(n-1)/2} + 1 > 0 \qquad \text{for} \quad 0 < \alpha < 1$$

So $f(\alpha)$ has a unique root between 0 and 1.

To find D, note that

$$l\sqrt{\frac{r_0 c_0}{R_D C_L}}\alpha^{(n+1)/2} + \alpha - 1 = 0$$

implies

$$\sqrt{R_D C_L} = l\sqrt{r_0 c_0}\frac{\alpha^{n+1/2}}{1-\alpha}.$$

Substituting $\sqrt{R_D C_L}$ into (16), we get

$$\begin{aligned} D &= \frac{r_0 c_0 L^2}{n^2}\frac{\alpha^{n+1}}{(1-\alpha)^2} + \frac{r_0 c_0 L^2}{2n} + \frac{r_0 c_0 L^2}{n^2}\frac{\alpha^{n+1} - n\alpha^2 + (n-1)\alpha}{(1-\alpha)^2} \\ &\quad + \frac{2 r_0 c_0 L^2}{n^2}\frac{\alpha(1-\alpha^n)}{(1-\alpha)^2} \\ &= \frac{r_0 c_0 L^2}{2n^2} \cdot \frac{n + 2\alpha - n\alpha^2}{(1-\alpha)^2}. \quad \square \end{aligned}$$

The results of Lemma 5 and Lemma 7 is summarized in the following theorem.

THEOREM 1. *For the optimal solution of the Wire Sizing problem (WS), we have*

$$\begin{aligned} l_i &= L/n && \text{for} \quad 1 \le i \le n \\ h_i &= \sqrt{\frac{r_0 C_L}{c_0 R_D}\frac{1}{\alpha^{n-1}}}\alpha^{i-1} && \text{for} \quad 1 \le i \le n \end{aligned}$$

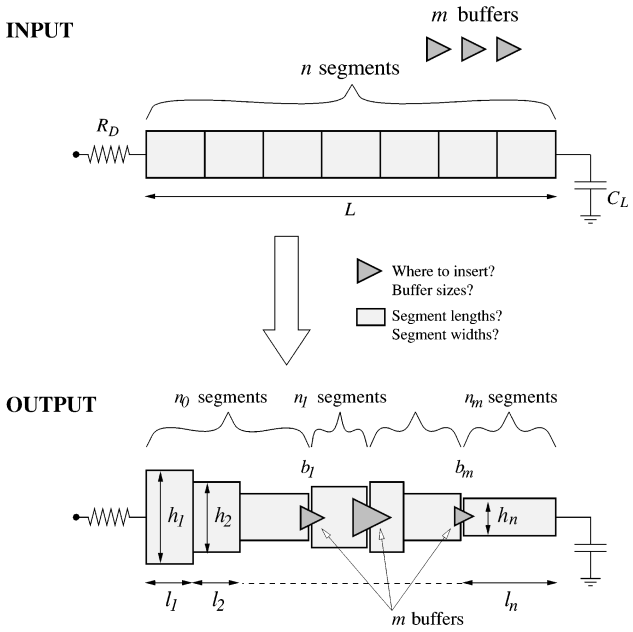

Fig. 5. Illustration of the problem BISWS/m. The input is L, R_D, C_L, n and m. The output is $n_0, \ldots, n_m$, $b_1, \ldots, b_m$, $l_1, \ldots, l_n$ and $h_1, \ldots, h_n$. We provide a closed form optimal solution of it which minimizes the delay.

$$D = \frac{r_0 c_0 L^2}{2n^2} \cdot \frac{n + 2\alpha - n\alpha^2}{(1-\alpha)^2}.$$

where α is the unique root between 0 and 1 of

$$f(\alpha) = \frac{L}{n}\sqrt{\frac{r_0 c_0}{R_D C_L}}\alpha^{(n+1)/2} + \alpha - 1.$$

5. SIMULTANEOUS BUFFER INSERTION/SIZING AND WIRE SIZING WITH m BUFFERS

In order to simplify the notations, we treat the driver and the load as buffers of fixed size in the rest of the paper. We call the driver the 0th buffer and the load the $(m+1)$th buffer. Let $b_0 = r_e/R_D$ and $b_{m+1} = C_L/c_g$. For $0 \le j \le m+1$, let $s_j = n_0 + \cdots + n_{j-1}$. In other words, s_j is the total number of segments between the driver and the jth buffer.

In this section, we consider the simultaneous Buffer Insertion/Sizing and Wire Sizing problem with m buffers (BISWS/m). In other words, we minimize D over $n_0, \ldots, n_m, b_1, \ldots, b_m, l_1, \ldots, l_n$ and $h_1, \ldots, h_n$. See Figure 5 for an illustration of BISWS/m.

Instead of considering BISWS/m directly, we first consider a restricted version of it such that m as well as $n_0, \ldots, n_m$ are fixed (with $n_0 + \cdots + n_m = n$). Note that if we consider the piece of wire between the jth buffer and the $(j+1)$th buffer, the sizing problem of it is similar to the one discussed in Section 4 with

n_j segments. However, the upstream resistance, which is r_e/b_j, and the downstream capacitance, which is $c_g b_{j+1}$, and the length of this piece are not fixed as we allow variables to be changed simultaneously. This complicates the problem a lot. In what follows, we exploit some interesting properties so that closed form optimal solution can be obtained.

The following lemma implies that even under buffer insertion and sizing, the wire should still be divided into equal length segments.

LEMMA 8. *For the optimal solution of BISWS/m with $n_0, \ldots, n_m$ fixed, $l_1 = l_2 = \cdots = l_n = L/n$.*

PROOF. For any j, consider the jth buffer, segment s_j and segment s_j+1 (i.e., the 2 segments around the jth buffer). Let $\hat{L} = l_{s_j} + l_{s_j+1}$. As in Lemma 5, we assume that $\hat{L}$ is fixed while l_{s_j} and l_{s_j+1} are considered as variables. Let $R_{\mathcal{U}}$ be the upstream resistance of segment s_j and $C_{\mathcal{D}}$ be the downstream capacitance of segment s_j+1. Note that $R_{\mathcal{U}}$ and $C_{\mathcal{D}}$ are independent of $b_j, h_{s_j}, h_{s_j+1}, l_{s_j}$ and l_{s_j+1}. By Lemma 3,

$$\begin{aligned} D &= \frac{r_0 c_0 l_{s_j}^2}{2} + 2 l_{s_j} \sqrt{r_0 c_0 R_{\mathcal{U}} (c_g b_j)} + R_{\mathcal{U}} (c_g b_j) \\ &\quad + \frac{r_0 c_0 l_{s_j+1}^2}{2} + 2 l_{s_j+1} \sqrt{r_0 c_0 C_{\mathcal{D}} \frac{r_e}{b_j}} + C_{\mathcal{D}} \frac{r_e}{b_j} + D', \end{aligned}$$

where D' are terms independent of $b_j, h_{s_j}, h_{s_j+1}, l_{s_j}$ and l_{s_j+1}.

Put $l_{s_j+1} = \hat{L} - l_{s_j}$ into D and let $\rho = \sqrt{r_0 c_0 r_e c_g}$, we can write

$$\begin{aligned} D &= r_0 c_0 l_{s_j}^2 + \left(2\rho \sqrt{\frac{R_{\mathcal{U}} b_j}{r_e}} - 2\rho \sqrt{\frac{C_{\mathcal{D}}}{c_g b_j}} - r_0 c_0 \hat{L} \right) l_{s_j} \\ &\quad + \left(\frac{r_0 c_0 \hat{L}^2}{2} + 2\hat{L}\rho \sqrt{\frac{C_{\mathcal{D}}}{c_g b_j}} + r_e c_g \left(\frac{R_{\mathcal{U}} b_j}{r_e} + \frac{C_{\mathcal{D}}}{c_g b_j} \right) + D' \right). \end{aligned}$$

This is a quadratic equation in l_{s_j}. By Lemma 2, D is minimized when

$$l_{s_j} = -\frac{2\rho \sqrt{R_{\mathcal{U}} b_j / r_e} - 2\rho \sqrt{C_{\mathcal{D}} / c_g b_j} - r_0 c_0 \hat{L}}{2 r_0 c_0}. \tag{17}$$

So

$$\begin{aligned} D &= \left(\frac{r_0 c_0 \hat{L}^2}{2} + 2\hat{L}\rho \sqrt{\frac{C_{\mathcal{D}}}{c_g b_j}} + r_e c_g \left(\frac{R_{\mathcal{U}} b_j}{r_e} + \frac{C_{\mathcal{D}}}{c_g b_j} \right) + D' \right) \\ &\quad - \frac{\left(2\rho \sqrt{R_{\mathcal{U}} b_j / r_e} - 2\rho \sqrt{C_{\mathcal{D}} / c_g b_j} - r_0 c_0 \hat{L} \right)^2}{4 r_0 c_0} \\ &= \frac{r_0 c_0 \hat{L}^2}{4} + \rho \left(\sqrt{\frac{R_{\mathcal{U}} b_j}{r_e}} + \sqrt{\frac{C_{\mathcal{D}}}{c_g b_j}} \right) \hat{L} + 2\sqrt{r_e c_g R_{\mathcal{U}} C_{\mathcal{D}}} + D'. \end{aligned}$$

Consider D as a function of $\sqrt{b_j}$. By Lemma 1, D is minimized when

$$b_j = \sqrt{\frac{C_{\mathcal{D}}}{c_g}} \Big/ \sqrt{\frac{R_{\mathcal{U}}}{r_e}},$$

or equivalently,

$$\sqrt{\frac{R_{\mathcal{U}} b_j}{r_e}} = \sqrt{\frac{C_{\mathcal{D}}}{c_g b_j}}.$$

So according to (17), $l_{s_j} = \hat{L}/2$. Therefore, $l_{s_j+1} = l_{s_j}$. This together with Lemma 5 implies $l_1 = l_2 = \cdots = l_n = L/n$ for the optimal solution. □

By Lemma 6, we know $h_{s_j+1}, h_{s_j+2}, \ldots, h_{s_{(j+1)}}$ form a geometric progression for each $0 \le j \le m$. Let α_j be the constant such that $h_{s_j+i} = h_{s_j+1}{\alpha_j}^{i-1}$ for $1 \le i \le n_j$. By Lemma 4, we know that $0 < \alpha_j < 1$ for $0 \le j \le m$. The following lemma proves the surprising result that the constants α_j's corresponding to different wire sizing problem instances between any two buffers are all the same.

LEMMA 9. *For the optimal solution of BISWS/m with $n_0, \ldots, n_m$ fixed, $\alpha_0 = \alpha_1 = \cdots = \alpha_m$.*

PROOF. Let $l = L/n$. By Lemma 8, $l_i = l$ for $1 \le i \le n$. In this proof, we treat α_{j-1} and α_j, and hence D, as functions of b_j for some j. We minimize D with respect to b_j but we write the optimality condition in terms of α_{j-1} and α_j.

Note that the sizing of the pieces of wires between two adjacent buffers are instances of WS. So by Theorem 1,

$$l\sqrt{\frac{r_0 c_0}{(r_e/b_{j-1})(c_g b_j)}}\alpha_{j-1}^{n_{j-1}+1/2} + \alpha_{j-1} - 1 = 0$$

or equivalently,

$$\frac{\alpha_{j-1}^{n_{j-1}+1}}{(1-\alpha_{j-1})^2} = \frac{r_e c_g}{r_0 c_0 l^2}\frac{b_j}{b_{j-1}}.$$

Differentiate with respect to b_j,

$$\begin{aligned}\frac{\alpha_{j-1}^{n_{j-1}}(n_{j-1}+1+\alpha_{j-1}-n_{j-1}\alpha_{j-1})}{(1-\alpha_{j-1})^3}\frac{d\alpha_{j-1}}{db_j} &= \frac{r_e c_g}{r_0 c_0 l^2}\frac{1}{b_{j-1}} \\ &= \frac{\alpha_{j-1}^{n_{j-1}+1}}{(1-\alpha_{j-1})^2}\frac{1}{b_j}.\end{aligned}$$

Hence

$$\frac{d\alpha_{j-1}}{db_j} = \frac{\alpha_{j-1}(1-\alpha_{j-1})}{n_{j-1}+1+\alpha_{j-1}-n_{j-1}\alpha_{j-1}}\frac{1}{b_j}.$$

Similarly, by Theorem 1,

$$l\sqrt{\frac{r_0c_0}{(r_e/b_j)(c_gb_{j+1})}}\alpha_j^{n_j+1/2}+\alpha_j-1\ =\ 0,$$

or equivalently,

$$\frac{\alpha_j^{n_j+1}}{(1-\alpha_j)^2}\ =\ \frac{r_ec_g}{r_0c_0l^2}\frac{b_{j+1}}{b_j}.$$

Differentiate with respect to b_j,

$$\begin{aligned}\frac{\alpha_j^{n_j}(n_j+1+\alpha_j-n_j\alpha_j)}{(1-\alpha_j)^3}\frac{d\alpha_j}{db_j}\ &=\ -\frac{r_ec_g}{r_0c_0l^2}\frac{b_{j+1}}{b_j^2}\\ &=\ -\frac{\alpha_j^{n_j+1}}{(1-\alpha_j)^2}\frac{1}{b_j}.\end{aligned}$$

Hence

$$\frac{d\alpha_j}{db_j}\ =\ -\frac{\alpha_j(1-\alpha_j)}{n_j+1+\alpha_j-n_j\alpha_j}\frac{1}{b_j}.$$

Let

$$D_j\ =\ \frac{r_0c_0l^2}{2}\frac{n_j+2\alpha_j-n_j\alpha_j^2}{(1-\alpha_j)^2}.$$

Then by Theorem 1,

$$D\ =\ mr_ec_d+\sum_{j=0}^{m}D_j.$$

Note that only D_{j-1} and D_j are dependent on b_j.

$$\begin{aligned}D\ &=\ \frac{r_0c_0l^2}{2}\frac{n_{j-1}+2\alpha_{j-1}-n_{j-1}\alpha_{j-1}^2}{(1-\alpha_{j-1})^2}+\frac{r_0c_0l^2}{2}\frac{n_j+2\alpha_j-n_j\alpha_j^2}{(1-\alpha_j)^2}\\ &\quad+\text{terms independent of } b_j,\\ \frac{dD}{db_j}\ &=\ \frac{r_0c_0l^2}{2}\left(\frac{2-2n_{j-1}\alpha_{j-1}}{(1-\alpha_{j-1})^2}+\frac{2\left(n_{j-1}+2\alpha_{j-1}-n_{j-1}\alpha_{j-1}^2\right)}{(1-\alpha_{j-1})^3}\right)\frac{d\alpha_{j-1}}{db_j}\\ &\quad+\frac{r_0c_0l^2}{2}\left(\frac{(2-2n_j\alpha_j)}{(1-\alpha_j)^2}+\frac{2\left(n_j+2\alpha_j-n_j\alpha_j^2\right)}{(1-\alpha_j)^3}\right)\frac{d\alpha_j}{db_j}\\ &=\ r_0c_0l^2\frac{n_{j-1}+1+\alpha_{j-1}-n_{j-1}\alpha_{j-1}}{(1-\alpha_{j-1})^3}\cdot\frac{d\alpha_{j-1}}{db_j}\\ &\quad+r_0c_0l^2\frac{n_j+1+\alpha_j-n_j\alpha_j}{(1-\alpha_j)^3}\cdot\frac{d\alpha_j}{db_j}\\ &=\ \frac{r_0c_0l^2}{b_j}\left(\frac{\alpha_{j-1}}{(1-\alpha_{j-1})^2}-\frac{\alpha_j}{(1-\alpha_j)^2}\right)\end{aligned}$$

$$\begin{aligned}
\frac{d^2D}{db_j^2} &= -\frac{r_0c_0l^2}{{b_j}^2}\left(\frac{\alpha_{j-1}}{(1-\alpha_{j-1})^2}-\frac{\alpha_j}{(1-\alpha_j)^2}\right)\\
&\quad+\frac{r_0c_0l^2}{b_j}\left(\left(\frac{1}{(1-\alpha_{j-1})^2}+\frac{2\alpha_{j-1}}{(1-\alpha_{j-1})^3}\right)\frac{d\alpha_{j-1}}{db_j}\right.\\
&\qquad\left.-\left(\frac{1}{(1-\alpha_j)^2}+\frac{2\alpha_j}{(1-\alpha_j)^3}\right)\frac{d\alpha_j}{db_j}\right)\\
&= -\frac{1}{b_j}\frac{dD}{db_j}+\frac{r_0c_0l^2(1+\alpha_{j-1})\alpha_{j-1}}{b_j^2(1-\alpha_{j-1})^2(n_{j-1}+1+\alpha_{j-1}-n_{j-1}\alpha_{j-1})}\\
&\quad+\frac{r_0c_0l^2(1+\alpha_j)\alpha_j}{b_j^2(1-\alpha_j)^2(n_j+1+\alpha_j-n_j\alpha_j)}\\
&> 0 \qquad \text{when } \frac{dD}{db_j}=0.
\end{aligned}$$

Therefore

$$\begin{aligned}
D \text{ is minimized} &\Leftrightarrow \frac{dD}{db_j}=0\\
&\Leftrightarrow \frac{\alpha_{j-1}}{(1-\alpha_{j-1})^2}-\frac{\alpha_j}{(1-\alpha_j)^2}=0\\
&\Leftrightarrow (\alpha_{j-1}\alpha_j-1)(\alpha_j-\alpha_{j-1})=0\\
&\Leftrightarrow \alpha_{j-1}=\alpha_j \quad \text{since } \alpha_{j-1}\alpha_j-1<0.
\end{aligned}$$

In other words, for the optimal solution, $\alpha_0=\alpha_1=\cdots=\alpha_m$. □

With Lemma 8 and Lemma 9, we are able to write b_j's, h_i's and D in closed form in the following lemma.

LEMMA 10. *For the optimal solution of BISWS/m with $n_0,\ldots,n_m$ fixed, we have*

$$\begin{aligned}
b_j &= b_0\frac{\alpha^{s_j}}{\beta^j} \qquad \textit{for} \quad 1\le j\le m\\
h_i &= \sqrt{\frac{r_0C_L}{c_0R_D}\frac{\beta^m}{\alpha^{n-1}}}\frac{\alpha^{i-1}}{\beta^j} \qquad \textit{for} \quad 1\le i\le n\\
&\quad \textit{with } j \textit{ being the index such that } s_j+1\le i\le s_{j+1}\\
&\quad (\textit{i.e., the } i\textit{th segment is between the } j\textit{th and } (j+1)\textit{th buffers})\\
D &= mr_ec_d+\frac{r_0c_0L^2}{2n^2}\cdot\frac{n+2(m+1)\alpha-n\alpha^2}{(1-\alpha)^2},
\end{aligned}$$

where $S=r_0c_0L^2/r_ec_gn^2$, α is the unique root between 0 and 1 of $g(\alpha)=\sqrt{b_0/b_{m+1}}\,S^{(m+1)/2}\,\alpha^{(n+m+1)/2}-(1-\alpha)^{m+1}$, and $\beta=(1-\alpha)^2/S\alpha$.

PROOF. By Lemma 9, let $\alpha_0=\alpha_1=\cdots=\alpha_m=\alpha$. Let $l=L/n$. By Lemma 8, $l_i=l$ for $1\le i\le n$. Note that the sizing of the pieces of wires between two

adjacent buffers are instances of WS. So by Theorem 1,

$$
\begin{aligned}
& l\sqrt{\frac{r_0 c_0}{(r_e/b_j)(c_g b_{j+1})}}\alpha^{(n_j+1)/2} + \alpha - 1 = 0 \qquad \text{for} \quad 0 \le j \le m \\
& \Rightarrow \sqrt{\frac{b_j}{b_{j+1}}}\alpha^{(n_j+1)/2} = \sqrt{\frac{1}{S}}(1-\alpha) \qquad \text{for} \quad 0 \le j \le m \qquad (18) \\
& \Rightarrow \prod_{j=0}^{m}\sqrt{\frac{b_j}{b_{j+1}}}\alpha^{(n_j+1)/2} = \prod_{j=0}^{m}\sqrt{\frac{1}{S}}(1-\alpha) \\
& \Rightarrow \sqrt{\frac{b_0}{b_{m+1}}}\alpha^{(n+m+1)/2} = \left(\frac{1}{S}\right)^{(m+1)/2}(1-\alpha)^{m+1}.
\end{aligned}
$$

Let

$$
g(\alpha) = \sqrt{\frac{b_0}{b_{m+1}}}S^{(m+1)/2}\alpha^{(n+m+1)/2} - (1-\alpha)^{m+1}.
$$

Then the optimal value of α which minimizes D is a root of $g(\alpha)$ between 0 and 1. Note that

$$
g(0) < 0 < g(1)
$$

and

$$
\begin{aligned}
g'(\alpha) &= \sqrt{\frac{b_0}{b_{m+1}}}S^{(m+1)/2}\frac{n+m+1}{2}\alpha^{(n+m+1)/2-1} + (m+1)(1-\alpha)^m \\
&> 0 \qquad \text{for} \quad 0 < \alpha < 1
\end{aligned}
$$

So $g(\alpha)$ has a unique root between 0 and 1.

Let $\beta = (1-\alpha)^2/S\alpha$. For b_j's, by (18),

$$
b_{k+1} = b_k\frac{S\alpha^{n_k+1}}{(1-\alpha)^2} = b_k\frac{\alpha^{n_k}}{\beta}.
$$

So

$$
\begin{aligned}
b_j &= b_0\left(\prod_{k=0}^{j-1}\frac{\alpha^{n_k}}{\beta}\right) \\
&= b_0\frac{\alpha^{s_j}}{\beta^j}.
\end{aligned}
$$

For h_i's, by Theorem 1, for $0 \le j \le m$ and $s_j + 1 \le i \le s_{j+1}$,

$$
\begin{aligned}
h_i &= \sqrt{\frac{r_0(c_g b_{j+1})}{c_0(r_e/b_j)}\frac{1}{\alpha^{n_j-1}}}\alpha^{i-s_j-1} \\
&= \sqrt{\frac{r_0 c_g}{c_0 r_e}b_j b_{j+1}\frac{1}{\alpha^{n_j-1}}}\alpha^{i-s_j-1}.
\end{aligned}
$$

Since $b_j = b_0\alpha^{s_j}/\beta^j$ and

$$\begin{aligned} b_{j+1} &= b_0\frac{\alpha^{s_{j+1}}}{\beta^{j+1}} = b_0\frac{\alpha^{s_{m+1}}}{\beta^{m+1}}\cdot\frac{\alpha^{s_{j+1}-s_{m+1}}}{\beta^{j-m}} = b_{m+1}\frac{\alpha^{s_{j+1}-n}}{\beta^{j-m}}, \\ h_i &= \sqrt{\frac{r_0c_g}{c_0r_e}b_0\frac{\alpha^{s_j}}{\beta^j}b_{m+1}\frac{\alpha^{s_{j+1}-n}}{\beta^{j-m}}\frac{1}{\alpha^{n_j-1}}}\alpha^{i-s_j-1} \\ &= \sqrt{\frac{r_0c_g}{c_0r_e}\frac{r_e}{R_D}\frac{C_L}{c_g}\frac{\alpha^{2s_j+n_j-n}}{\beta^{2j-m}}\frac{1}{\alpha^{n_j-1}}}\alpha^{i-s_j-1} \\ &= \sqrt{\frac{r_0C_L}{c_0R_D}\frac{\beta^m}{\alpha^{n-1}}}\frac{\alpha^{i-1}}{\beta^j}. \end{aligned}$$

For D, by Theorem 1,

$$\begin{aligned} D &= mr_ec_d + \sum_{j=0}^{m}\frac{r_0c_0L^2}{2n^2}\cdot\frac{n_j+2\alpha-n_j\alpha^2}{(1-\alpha)^2} \\ &= mr_ec_d + \frac{r_0c_0L^2}{2n^2}\cdot\frac{n+2(m+1)\alpha-n\alpha^2}{(1-\alpha)^2}. \quad \square \end{aligned}$$

Notice that by Lemma 10, the optimal delay D is independent of $n_0,\ldots,n_m$. That means we can set $n_0,\ldots,n_m$ arbitrarily (with the constraint that $n_0+\cdots+n_m=n$) without affecting the optimal delay. This observation together with Lemma 8 and Lemma 10 give the following theorem.

THEOREM 2. *For the optimal solution of the simultaneous Buffer Insertion/Sizing and Wire Sizing problem with m buffers* (*BISWS/m*), *we have*

$$\begin{aligned} n_j &= \text{an arbitrary nonnegative integer, for } 0\le j\le m \\ &\quad (\text{such that } n_0+\cdots+n_m=n) \\ b_j &= \frac{r_e}{R_D}\frac{\alpha^{s_j}}{\beta^j} \qquad \text{for} \quad 1\le j\le m \\ l_i &= L/n \qquad \text{for} \quad 1\le i\le n \\ h_i &= \sqrt{\frac{r_0C_L}{c_0R_D}\frac{\beta^m}{\alpha^{n-1}}}\frac{\alpha^{i-1}}{\beta^j} \qquad \text{for} \quad 1\le i\le n \\ &\quad \text{with } j \text{ being the index such that } s_j+1\le i\le s_{j+1} \\ &\quad (\text{i.e., the } i\text{th segment is between the } j\text{th and } (j+1)\text{th buffers}) \\ D &= mr_ec_d + \frac{r_0c_0L^2}{2n^2}\cdot\frac{n+2(m+1)\alpha-n\alpha^2}{(1-\alpha)^2} \end{aligned}$$

where $S = r_0c_0L^2/r_ec_gn^2$, $s_j = n_0+\cdots+n_{j-1}$, α *is the unique root between* 0 *and* 1 *of*

$$g(\alpha) = \sqrt{\frac{r_ec_g}{R_DC_L}}S^{(m+1)/2}\alpha^{(n+m+1)/2} - (1-\alpha)^{m+1},$$

and $\beta = (1-\alpha)^2/S\alpha$.

6. SIMULTANEOUS BUFFER INSERTION/SIZING AND WIRE SIZING WITH OPTIMAL NUMBER OF BUFFERS

Now, we consider the problem BISWS. In other words, we minimize D over m, $n_0, \ldots, n_m$, $b_1, \ldots, b_m$, $l_1, \ldots, l_n$ and $h_1, \ldots, h_n$ simultaneously. (See Figure 1.) The optimal number of buffers m is given by the following lemma.

LEMMA 11. *For the optimal solution of BISWS, we have m equals the better one of* $\lfloor \hat{m} \rfloor$ *and* $\lceil \hat{m} \rceil$, *where*

$$\hat{m} = \left(\ln \frac{r_e c_g}{R_D C_L \beta} \left(1 + \frac{S\beta}{2} - \sqrt{S\beta + \left(\frac{S\beta}{2} \right)^2} \right)^n \right) \Big/ \ln \beta,$$

$S = r_0 c_0 L^2 / r_e c_g n^2$, *and* $(1/e\beta)^{1/\beta} = e^{c_d / c_g}$.

PROOF. By Theorem 2, if the number of buffers used is m, then for the optimal solution,

$$D = m r_e c_d + \frac{r_0 c_0 L^2}{2n^2} \cdot \frac{n + 2(m+1)\alpha - n\alpha^2}{(1-\alpha)^2}, \tag{19}$$

where

$$\sqrt{\frac{r_e c_g}{R_D C_L}} S^{(m+1)/2} \alpha^{(n+m+1)/2} - (1-\alpha)^{m+1} = 0,$$

or equivalently,

$$\frac{r_e c_g}{R_D C_L} \alpha^n = \beta^{m+1}. \tag{20}$$

Let $\beta = (1-\alpha)^2 / S\alpha$. Then

$$\begin{aligned} \frac{d\beta}{d\alpha} &= \frac{-2(1-\alpha)}{S\alpha} - \frac{(1-\alpha)^2}{S\alpha^2} \\ &= -\frac{(1-\alpha)(1+\alpha)}{S\alpha^2}. \end{aligned}$$

Differentiate (20) with respect to α,

$$\begin{aligned} \frac{r_e c_g}{R_D C_L} n \alpha^{n-1} &= \beta^{m+1} \cdot \left(\frac{d\beta}{d\alpha} \frac{m+1}{\beta} + \frac{dm}{d\alpha} \ln \beta \right), \\ \frac{dm}{d\alpha} &= \left(\frac{n}{\alpha} + \frac{(1-\alpha)(1+\alpha)}{S\alpha^2} \frac{m+1}{\beta} \right) \Big/ \ln \beta \\ &= \frac{n - n\alpha + (m+1) + (m+1)\alpha}{\alpha(1-\alpha)\ln \beta}. \end{aligned}$$

Differentiate (19) with respect to m, we get

$$\begin{aligned} \frac{dD}{dm} = r_e c_d + \frac{r_0 c_0 L^2}{2n^2} \Bigg(\Bigg(2(m+1)\frac{d\alpha}{dm} + 2\alpha - 2n\alpha \frac{d\alpha}{dm} \Bigg) \cdot \frac{1}{(1-\alpha)^2} \\ + (n + 2(m+1)\alpha - n\alpha^2) \cdot \frac{-2}{(1-\alpha)^3} \left(- \frac{d\alpha}{dm} \right) \Bigg) \end{aligned}$$

$$
\begin{aligned}
&= r_e c_d + \frac{r_0 c_0 L^2}{n^2} \cdot \left(\frac{n - n\alpha + (m+1) + (m+1)\alpha}{(1-\alpha)^3} \frac{d\alpha}{dm} + \frac{\alpha}{(1-\alpha)^2} \right) \\
&= r_e c_d + \frac{r_0 c_0 L^2}{n^2} \cdot \frac{\alpha}{(1-\alpha)^2} (\ln \beta + 1) \\
&= r_e c_d + r_e c_g \frac{\ln \beta + 1}{\beta}
\end{aligned}
$$

$$
\begin{aligned}
\frac{d^2 D}{dm^2} &= r_e c_g \left(\frac{1}{\beta^2} - \frac{\ln \beta + 1}{\beta^2} \right) \frac{d\beta}{dm} \\
&= -r_e c_g \frac{\ln \beta}{\beta^2} \frac{d\beta}{d\alpha} \frac{d\alpha}{dm} \\
&= r_e c_g \frac{(\ln \beta)^2}{\beta^2} \frac{(1-\alpha)^2 (1+\alpha)}{S\alpha(n - n\alpha + (m+1) + (m+1)\alpha)} \\
&> 0 \qquad \text{as } 0 < \alpha < 1.
\end{aligned}
$$

So D is a convex function with respect to m. Therefore

$$
\begin{aligned}
D \text{ is minimized} &\Leftrightarrow \frac{dD}{dm} = 0 \\
&\Leftrightarrow r_e c_d + r_e c_g \frac{\ln \beta + 1}{\beta} = 0 \\
&\Leftrightarrow -\frac{\ln \beta + 1}{\beta} = \frac{c_d}{c_g} \\
&\Leftrightarrow \left(\frac{1}{e\beta} \right)^{1/\beta} = e^{c_d / c_g}
\end{aligned}
$$

Since $\beta = (1-\alpha)^2 / S\alpha$, or equivalently, $\alpha^2 - (2 + S\beta)\alpha + 1 = 0$, and we know $0 < \alpha < 1$,

$$
\alpha = 1 + \frac{S\beta}{2} - \sqrt{S\beta + \left(\frac{S\beta}{2} \right)^2}.
$$

Take the logarithm of both sides of (20) and rearrange,

$$
\begin{aligned}
m &= \left(\ln \frac{r_e c_g}{R_D C_L} \alpha^n \right) \Big/ \ln \beta - 1 \\
&= \left(\ln \frac{r_e c_g}{R_D C_L \beta} \left(1 + \frac{S\beta}{2} - \sqrt{S\beta + \left(\frac{S\beta}{2} \right)^2} \right)^n \right) \Big/ \ln \beta.
\end{aligned}
$$

Suppose D is minimized when $m = \hat{m}$, where $\hat{m}$ is not necessary to be an integer. Since D is a convex function with respect to m, the integer value that minimizes D is either $\lfloor \hat{m} \rfloor$ or $\lceil \hat{m} \rceil$. □

Lemma 11 together with Theorem 2 give the following theorem.

THEOREM 3. *For the optimal solution of the simultaneous Buffer Insertion/Sizing and Wire Sizing problem (BISWS), we have*

$$m = \text{the better one of } \lfloor \hat{m} \rfloor \text{ and } \lceil \hat{m} \rceil,$$

where

$$S = \frac{r_0 c_0 L^2}{r_e c_g n^2},$$

$$\hat{m} = \left(\ln \frac{r_e c_g}{R_D C_L \hat{\beta}} \left(1 + \frac{S\hat{\beta}}{2} - \sqrt{S\hat{\beta} + \left(\frac{S\hat{\beta}}{2} \right)^2} \right)^n \right) \Big/ \ln \hat{\beta}, \quad \text{and}$$

$$\left(\frac{1}{e\hat{\beta}} \right)^{1/\hat{\beta}} = e^{c_d / c_g}.$$

Moreover,

$$\begin{aligned}
n_j &= \text{an arbitrary nonnegative integer, for } 0 \le j \le m \\
&\quad (\text{such that } n_0 + \cdots + n_m = n) \\
b_j &= \frac{r_e}{R_D} \frac{\alpha^{s_j}}{\beta^j} \qquad \text{for} \quad 1 \le j \le m \\
l_i &= \frac{L}{n} \qquad \text{for} \quad 1 \le i \le n \\
h_i &= \sqrt{\frac{r_0 C_L}{c_0 R_D} \frac{\beta^m}{\alpha^{n-1}}} \frac{\alpha^{i-1}}{\beta^j} \qquad \text{for} \quad 1 \le i \le n \\
&\quad \text{with } j \text{ being the index such that } s_j + 1 \le i \le s_{j+1} \\
&\quad (\text{i.e., the } i\text{th segment is between the } j\text{th and } (j+1)\text{th buffers}) \\
D &= m r_e c_d + \frac{r_0 c_0 L^2}{2n^2} \cdot \frac{n + 2(m+1)\alpha - n\alpha^2}{(1-\alpha)^2},
\end{aligned}$$

where $s_j = n_0 + \cdots + n_{j-1}$, α *is the unique root between* 0 *and* 1 *of*

$$g(\alpha) = \sqrt{\frac{r_e c_g}{R_D C_L}} S^{(m+1)/2} \alpha^{(n+m+1)/2} - (1-\alpha)^{m+1},$$

and $\beta = (1-\alpha)^2 / S\alpha$.

7. DISCUSSION

In this section, some interesting implications and extensions of our closed form solutions are presented. For the experiments in this section, we use the parameters of the 0.18 μm technology listed in Cong and Pan [1998], which is based on the 1997 National Technology Roadmap for Semiconductors (NTRS'97) [Semiconductor Industry Association 1997]. The values are shown in Table I. Buffers of size 200 $\times$ minimum device are used both as driver and as load.

7.1 Generalization of Previous Results

We observe that several previous results are special cases of our result.

Table I. Parameters of the 0.18 μm Technology Based on NTRS'97.

r_0	c_0	c_f	r_e	c_g	c_d	W_{min}
$0.0679\Omega/\square$	$0.0596fF/\mu m^2$	$0.0641fF/\mu m$	$17.1k\Omega$	$0.234fF$	$3.883fF$	$0.18\ \mu m$

c_f is the unit length wire fringing capacitance.
W_{min} is the minimum wire width.
All other parameters are defined in Section 3.

Wire sizing alone. In this paper, the wire is divided into a finite number of uniform-width segments. Therefore, the width function describing the optimal wire shape is a step function. In Chen et al. [1996b] and Fishburn and Schevon [1995], a continuous version of the wire sizing problem was considered. The wire was divided into an infinite number of segments. Therefore, the width function describing the optimal wire shape is a continuous function. These two papers proved that the optimal width function should be an exponential function. Note that by letting n tends to infinity, our result on WS (Theorem 1) implies their results.

Buffer sizing alone. If we ignore all the wire segments in Section 5 and Section 6 by setting $L = 0$ (i.e., $l_i = 0$ for all i), then our result on BISWS (Theorem 3) implies the results for the tapered buffer structure in Lin and Linholm [1975] and Jaeger [1975].

7.2 The Use of Equal-Length Segments

For previous papers which apply wire sizing for interconnect delay optimization, the problem formulations usually allow changing of segment widths while segment lengths are given as input. Some papers (e.g., Cong and He [1996] and Cong and Leung [1993]) made the assumption that the input segment lengths are all equal. Then they solved the problems of determining the wire widths by iterative algorithms. This is a very natural assumption to make, but no one actually proves that this is the best. In this paper, we consider a more general formulation by allowing the lengths of segments to be varied. However, we prove that for the optimal solution, the wire is always divided into equal length segments (no matter how many buffers we use and no matter where we put the buffers). That means using segments of different length does not have any advantage with respect to the delay. Therefore, our result justifies the assumption made in previous works.

7.3 Trade-off between Delay and Number of Segments Used

We point out in Section 1 that the number of segments used n is a parameter that allows us to determine the quality of the solution. We can get a smaller delay D by using a larger value of n. In order to suggest a good value of n to be used in practice, we take a 10000 μm long wire and apply our solution of BISWS to it using different values of n. Figure 6 plots D as a function of n. We also compute the delay corresponding to $n = 1000$, which is assumed to be the best possible value. If an accuracy of 2% within the best possible value is desired, a value of $n \geq 6$ is needed. If an accuracy of 0.2% is desired, a value of $n \geq 17$ is needed.

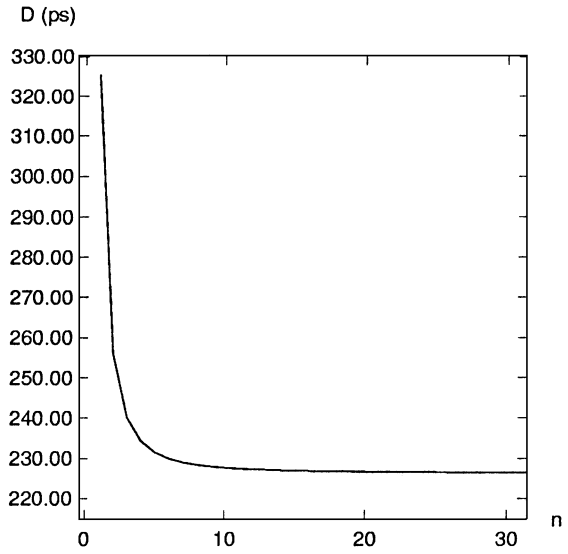

Fig. 6. The delay D versus the number of segments used n.

7.4 Minimizing Area subject to Bounds on Buffer Size and Wire Width

In Section 5, we pointed out that D in Theorem 2 is independent of $n_0, n_1, \ldots, n_m$. In other words, for any fixed number of buffers inserted, if the buffers and wires are allowed to be sized simultaneously and continuously, we can put the buffers anywhere between two adjacent segments without affecting the optimal delay. Note that although the delay is not affected by the buffer locations, other design objectives, such as total wire area, total power dissipation, minimum wire width or minimum buffer size, are very sensitive to buffer locations. So the flexibility in buffer locations can be used in optimizing other objectives. In this section, we demonstrate how this flexibility can be used to minimize buffer and wire area among minimum delay solutions such that the buffer sizes and wire widths are larger than some lower bounds.

We use a wire that is 15000 μm in length as an illustration. We set $m = 2$ (i.e., 2 buffers) and $n = 6$ (i.e., 6 segments). Since $0 \leq s_1 \leq s_2 \leq 6$, there are $7+6+\cdots+1 = 28$ optimal solutions of BISWS/m with different buffer locations. Four of the solutions are shown in Figure 7.

If the ith segment is between the jth buffer and the $(j+1)$th buffer (i.e., $s_j + 1 \leq i \leq s_{j+1}$), by Theorem 2, the size of the jth buffer b_j and the width of the ith wire h_i are given as follows.

$$b_j = \frac{r_e}{R_D} \frac{\alpha^{s_j}}{\beta^j} \tag{21}$$

$$h_i = \sqrt{\frac{r_0 C_L}{c_0 R_D} \frac{\beta^m}{\alpha^{n-1}}} \frac{\alpha^{i-1}}{\beta^j} \tag{22}$$

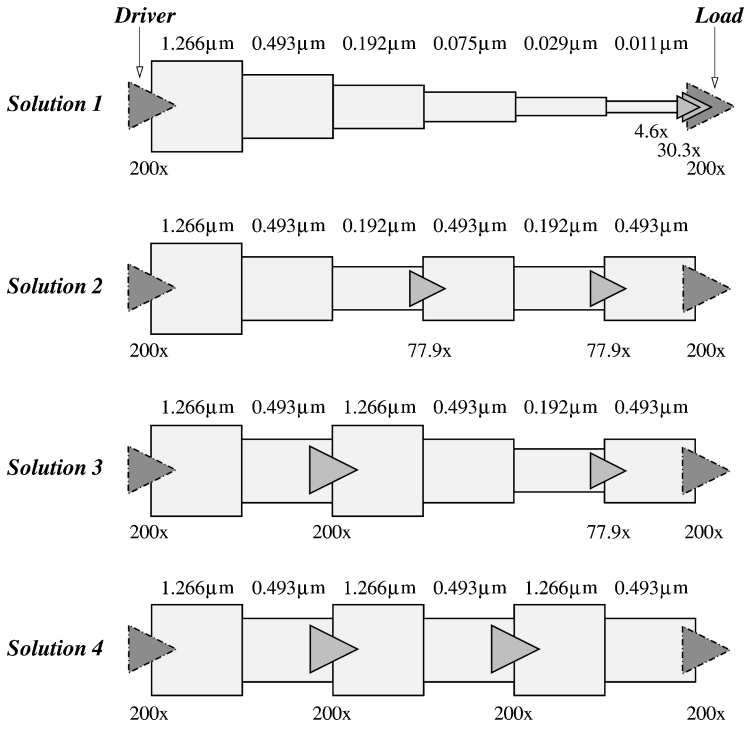

Fig. 7. Four optimal solutions of BISWS/m with different buffer locations. The segment widths are written above the segments. The buffer sizes are written as a ratio over the minimum device below the buffers.

We know that α is less than 1. β is also less than 1 in practice. (Note that $1/\beta$ is the buffer tapering factor if wire segments are ignored. If the optimal number of buffers is used, β can be proved to be less than 1.) Therefore, for any j, b_j is smaller if s_j (i.e., number of segments before the jth buffer) is larger. For any i, h_i is smaller if j (i.e., number of buffers before the ith segment) is larger. In other words, if we cascade all buffers just before the load (i.e., $s_1 = \cdots = s_m = n$), then both the buffer area and the wire area will be minimized. For the problem in Figure 7, Solution 1 is the one with minimum buffer and wire area.

However, for the minimum-area solution, buffers may be too small and wire segments may be too narrow. So instead of using $s_j = n$, we use the largest s_j such that the solution is still above the bounds. In the following, the way to find the largest feasible s_j is discussed. Suppose the jth buffer is just after the ith segment. Note that if we decrease s_j by one (i.e., we move the jth buffer from just after the ith segment to just before the ith segment), by (22) and (21), all buffer sizes and all segment widths will remain the same except for the jth buffer and the ith segment. The size of the jth buffer b_j will be divided by a factor α, and the width of the ith segment h_i will be divided by a factor β. In other words, both the size of the jth buffer and the width of the ith segment

will be increased if s_j is decreased by one. For an illustration, compare Solution 2 and Solution 3 in Figure 7, in which the first buffer is moved across the third segment from Solution 2 to Solution 3.

The algorithm for determining buffer locations such that the buffer area and wire area are minimized and the buffer sizes and wire widths are larger than some given lower bounds can be summarized as follows:

Algorithm to Determine Buffer Locations

1. Set $s_j := n$ for $1 \leq j \leq m$.
2. Compute b_1 and h_{s_1} using Theorem 2.
3. **for** $j := 1$ **to** m **do**
   while b_j or h_{s_j} is below the lower bound **do**
   Set $s_j := s_j - 1$.
   Compute b_j and h_{s_j} using Theorem 2.
4. Place the jth buffer just after the s_jth segment for $1 \leq j \leq m$.

If we apply the algorithm to the problem in Figure 7, Solution 2 is obtained. For comparison, if the buffers are placed evenly along the wire, Solution 4 is obtained. We notice that Solution 4 uses 156.7% more buffer area and 68.6% more wire area than Solution 2.

7.5 Wire Fringing Capacitance Consideration

In this section, we present some experimental results on approximating the case with fringing capacitance by our closed, form solutions. We use wires the lengths of which range from 1000 μm to 20 000 μm and we set $n = 10$. For a wire of length L, we add half of the total fringing capacitance to the load (i.e., we add $c_f L/2$ to C_L). Then we obtain the solution of BISWS by Theorem 3. We notice that when fringing capacitance is considered, the delay is affected by the buffer locations. So we choose the best one among all n^m possible buffer placements of the solution of BISWS, where m is the number of buffers used. Note that it is very efficient to try all n^m buffer placements as m is usually small in practice. When the wire length is from 1000 μm to 5000 μm, from 6000 μm to 13 000 μm, and from 14 000 μm to 20 000 μm, m is zero, one, and two respectively. The delay of our solution and of the optimal solution (obtained by an iterative algorithm) are plotted in Figure 8.

In general, the accuracy of our solution is higher for shorter wires. If the wire length is within 8000 μm, our solution is within 2% of the optimal solution. Even for a wire of length 20 000 μm, our solution is only 3.5% away from the optimal solution.

Recently, Cong and Pan [1998] also derived a closed-form delay estimation model for an interconnect wire. In their model, fringing capacitance is taken into consideration. About 90% accuracy on average was reported.

Fringing capacitance will become more important as wires will become narrower. For future research, it would be nice if closed-form optimal solutions can be obtained even if fringing capacitance is considered. However, the closed-form solution is expected to be much more complicated. For example, the lengths of segments will no longer be equal and the widths of segments will no longer form a geometric progression in the optimal solution.

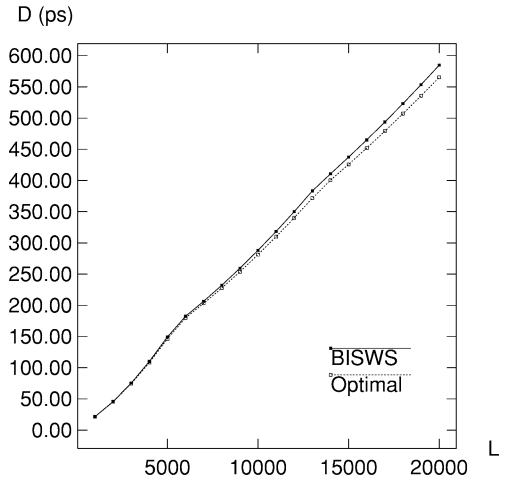

Fig. 8. Comparison of the approximate solution of BISWS and the optimal solution (obtained by an iterative algorithm) when fringing capacitance is considered.

7.6 Handling Interconnect Trees

For interconnect trees, minimizing maximum sink delay and minimizing total area subject to sink delay bounds are the most commonly used objectives. Chen et al. [1996] showed that both objectives can be reduced by the Lagrangian relaxation technique to a sequence of subproblems minimizing a weighted sum of the sink delays. In other words, by solving the problem of minimizing weighted sink delay, we also solve the problems of minimizing maximum sink delay and minimizing total area subject to sink delay bounds as well. So we consider the problem of minimizing weighted sink delay in the following.

To minimize a weighted sum of the sink delays of an interconnect tree, a similar technique as in Chen et al. [1996] can be used. The basic idea is to iteratively optimize the tree edges one at a time. In each iteration, we manipulate the tree edges one by one in a depth-first order. When an edge is manipulated, we keep all the other edges fixed and apply our closed form solutions to that edge. This method should be much faster and use much less memory than an iterative algorithm which divides each tree edge into several segments and locally sizes one segment at each step.

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