EE 330
Integrated Electronics
Spring 2014
COURSE INFORMATION

Room: Lecture - 0268 Carver (All Sections)
      Labs - 2046 Coover

Time: Lecture - MWF 9:00am-9:50am
      Laboratory - Section A: Tuesday 8:00am to 10:50am
                      Section B: Cancelled
                      Section C: Thursday 3:10pm to 6:00pm
                      Section D: Wednesday 3:10pm to 6:00pm
                      Section E: Friday 1:10pm to 4:00pm
                      Section F: Friday 10:00am to 12:50pm
                      Section G: Cancelled

Lecture Instructor:
Ayman Fayed
2117 Coover Hall
Voice: 515-294-6112
e-mail: aafayed@iastate.edu
Office Hours: Mondays and Wednesdays 10:30am to 11:30am, or appointments

Laboratory Instructors:
Wenbing Ma <mwb1992@iastate.edu>                             Sections: A, D
Craig Gustafson <craigg@iastate.edu>                           Sections: C, E
Yunxi Guo <yunxig@iastate.edu>                                Sections: F, HW Grading

Course Description:
Semiconductor technology for integrated circuits. Modeling of integrated devices
including diodes, BJTs, and MOSFETs. Physical layout. Circuit simulation. Digital building
blocks and digital circuit synthesis. Analysis and design of analog building blocks. Laboratory
exercises and design projects with CAD tools and standard cells.

Course Web Site: http://home.engineering.iastate.edu/~aafayed/ee330/
Homework assignments, lecture notes, laboratory assignments, and other course support
materials will be posted on this WEB site. Students will be expected to periodically check the
WEB site for information about the course.
Required Texts:

**CMOS VLSI Design – A Circuits and Systems Perspective, Fourth Edition**
by N. Weste and D. Harris, Addison Wesley, 2011

Reference Texts:

**Microelectronic Circuits (5th Edition)**
by Sedra and Smith, Oxford, 2004

**Digital Integrated Circuits (2nd Edition)**
by Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, Prentice Hall, 2002

**CMOS Circuit Design, Layout, and Simulation (2nd Edition)**

**Analog Integrated Circuit Design**

**Principles of CMOS VLSI Design**
by N. Weste and K. Eshraghian, Addison Wesley, 1992

**VLSI Design Techniques for Analog and Digital Circuits**

**CMOS Analog Circuit Design**
by Allen and Holberg, HRW, 2002.

**Design of Analog CMOS Integrated Circuits**
by B. Razavi, McGraw Hill, 1999

**The Art of Analog Layout**
by Alan Hastings, Prentice Hall, 2001

**CMOS IC Layout**
by Dan Cline, Newnes, 1999.

**Design of Analog Integrated Circuits**
by Laker and Sansen, McGraw Hill, 1994

**Analysis and Design of Analog Integrated Circuits-Fourth Edition**
Gray,Hurst, Lewis and Meyer, Wiley, 2001

**Analog MOS Integrated Circuits for Signal Processing**
Gregorian and Temes, Wiley, 1986
**Grading:**
Points will be allocated for several different parts of the course. A letter grade will be assigned based upon the total points accumulated. The points allocated for different parts of the course are as listed below:

- 3 Exams 100 pts total
- 1 Final 100 pts
- Homework 100 pts total
- Quizzes/Attendance 100 pts total
- Lab and Lab Reports 100 pts total
- Design Project (tentative) 100 pts

**Laboratory:**
There will be weekly lab experiments. A separate lab handout will be provided and will discuss lab procedures. Each missed lab session will deduct 50 points from your total course points (in addition to receiving a zero grade for the report of the missed lab session). Therefore, missing two lab sessions will entail losing the 100 points allocated for the lab portion of the course even if you complete the rest of the lab sessions. Missing more than two lab sessions will effectively erase the points you score in other portions of the course and may inevitably lead to failing the course regardless of your performance in the other portions of the course. If a legitimate and convincing excuse is provided for missing a lab session, you are expected to independently perform the lab and submit its report to your lab TA BEFORE your next lab session in order to receive credit for it and avoid the penalty. Lab reports are due to your Lab TA at the beginning of your next lab session. No late reports will be accepted without a legitimate excuse. TAs are instructed not to accept any late lab reports. If you have an excuse you must talk to me in person.

**Project:**
A design project will be assigned towards the end of the course. A separate document describing the projects and the policy will be posted towards the end of the course.

**Homework:**
Homework assignments are due at the beginning of the class period on the designated due dates. No late homework will be accepted without an acceptable excuse. Please note that TAs are instructed not to accept any HW submission. The HW must be submitted to me personally.

**Lecture Attendance:**
At the beginning of each Lecture, the instructor will call out 5 or more random names. If your name is called and you are not present, you will lose 25 points from the 100 points allocated for attendance. Therefore, missing 4 lectures will entail losing the 100 points allocated to class attendance. Missing more than 4 classes will NOT impose any further deduction of points. If your name is called once and you are not present, the instructor may choose to repeat calling your name in next lectures. If a legitimate and convincing excuse is provided for missing a lecture, the loss of credit for attendance may be reconsidered.

Last updated 01/03/2014
Participation:
Participation in all class functions and provisions for special circumstances will be in accord with ISU policy. Attendance of any classes or labs, turning in of homework, or taking any exams or quizzes is optional; however grades will be assigned in accord with grading policy described above, particularly for the lab and attendance.

Academic Dishonesty:
Any academic dishonesty will not be tolerated. This includes copying lab reports, project reports, or homework solutions from others, whether from the same semester or from previous semesters. It also includes any attempts to claim attendance for someone else during lecture. Any detected dishonesty will be treated in accordance to ISU standards and procedures.