EE330
Integrated Electronics
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Devices in Semiconductor Processes

Resistors, Diodes, Capacitors, MOSFETs, BJTs
Basic Semiconductor Processes

- There are several semiconductor processes, each has a primary device that it implements along with other secondary devices.

- The Metal Oxide Semiconductor (MOS) Process
  - Primary device → The MOSFET
  - Niche device → The MESFET
  - Secondary devices → Diode, Resistor, Capacitor, BJT, Schottky Diode

- There are different flavors of MOS Processes
  - NMOS Process → Contains only n-channel MOS devices
  - PMOS Process → Contains only p-channel MOS devices
  - CMOS Process → Contains both n-channel and p-channel MOS devices
There are several semiconductor processes, each has a primary device that it implements along with other secondary devices.

The Bipolar Process
- Primary device → The BJT (Bipolar Junction Transistor)
- Niche device → The HBJT or HBT (Heterojunction Bipolar Junction Transistor)
- Secondary devices → Diode, Resistor, Capacitor, Schottky Diode, JFET (Junction Field Effect Transistor)

There are different flavors of Bipolar Processes
- T^2L → Transistor-Transistor Logic → Digital
- ECL → Emitter-Coupled Logic → High speed digital
- I^2L → Integrated Injection Logic → Low power digital
- Linear ICs → Analog and Linear Circuits
Basic Semiconductor Processes

- There are several semiconductor processes, each has a primary device that it implements along with other secondary devices.

- Thin and Thick Film Processes
  - Primary Device: The Resistor

- BiMOS or BiCMOS \(\rightarrow\) Combines MOS and Bipolar Devices
  - Primary Devices: MOSFET & BJT

- SiGe \(\rightarrow\) BJT with HBT implementation

- SiGe / MOS \(\rightarrow\) Combines HBT & MOSFET technology

- SOI / SOS (Silicon on Insulator / Silicon on Sapphire)

- Twin-Well & Twin-Tub CMOS
  - Very similar to basic CMOS but more optimal transistor characteristics
Basic Semiconductor Processes

◆ **Standard CMOS Process**
  - MOS Transistors → n-channel and p-channel
  - Resistors, Capacitors, Diodes
  - BJT → Decent in some processes → PNP and NPN, but PNP is more common
  - JFET → In some processes → n-channel and p-channel

◆ **Standard Bipolar Process**
  - BJT → PNP and NPN
  - Resistors, Capacitors, Diodes
  - JFET → n-channel and p-channel

◆ **Niche Devices**
  - Photodetectors (photodiodes, phototransistors, photoresistors)
  - MESFET, HBT, Schottky Diode (not Shockley), MEM Devices, TRIAC/SCR
Basic Semiconductor Processes

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- MOS Transistors → n-channel and p-channel
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- MESFET, HBT, Schottky Diode (not Shockley), MEM Devices, **TRIAC/SCR**
Basic Devices

- Resistor
- Diode
- Capacitor
- MOSFET
- BJT
Basic Devices: Resistors

- Generally thin-film devices

- Almost any thin-film layer can be used as a resistor
  - Diffused resistors
  - Poly Resistors
  - Metal Resistors

- Subject to process variations, gradient effects and local random variations

- Often temperature and voltage dependent
  - Ambient temperature
  - Local Heating due to current flow

- Nonlinearities often a cause of distortion when used in circuits

- Trimming may be possible
  - Laser, links, and switches
Basic Devices: Resistors

**Resistor Model**

\[ R = \frac{V}{I} \]
Basic Devices: Resistors

- **Resistivity** → Volumetric measure of conduction capability of a material → Measured in (Ω.cm)
- For homogeneous material, resistivity is independent of geometry (A, L)

\[ R = \frac{L}{A}\rho \]
Basic Devices: Resistors

- For thin film material ($d \ll W, d \ll L$) → We use sheet resistance instead of resistivity.
- Sheet resistance is independent of $W$ and $L$, but it is a function of the thickness $H$.

\[
R = \frac{L}{A} = \frac{L}{W \left[ \frac{\rho}{H} \right]}
\]

Define $R_{\square} = \frac{\rho}{H}$ → Sheet Resistance (measured in Ω or also in Ω/□)

Define $N_S = \frac{L}{W}$ → Number of Squares

\[
R = R_{\square} \times N_S
\]
Basic Devices: Resistors

- Resistivity of various materials used in semiconductor processing
  - Cu $\rightarrow 1.7E-6 \ \Omega\cdot cm$
  - Al $\rightarrow 2.7E-4 \ \Omega\cdot cm$
  - Gold $\rightarrow 2.4E-6 \ \Omega\cdot cm$
  - Platinum $\rightarrow 3.0E-6 \ \Omega\cdot cm$
  - n-Si $\rightarrow 0.25$ to $5 \ \Omega\cdot cm$
  - Intrinsic Si $\rightarrow 2.5E5 \ \Omega\cdot cm$
  - SiO$_2$ $\rightarrow 1E14 \ \Omega\cdot cm$
Resistor Nonidealities: Temperature Coefficient

- Used to quantify how a resistor may change with temperature

\[ TCR = 10^6 \times \left( \frac{1}{R} \frac{dR}{dT} \right) \bigg|_{\text{op. temp}} \] (Measured in ppm/°C)

- If TCR is Constant

\[ R(T_2) = R(T_1) e^{\frac{T_2 - T_1}{10^6} TCR} \approx R(T_1) \left[ 1 + (T_2 - T_1) \frac{TCR}{10^6} \right] \]

- Capacitor variations with temperature can be described by the same equation by replacing the resistance with the capacitance
Resistor Nonidealities: Voltage Coefficients

- Used to quantify how a resistor may change with the voltage across it

\[
VCR = 10^6 \times \left( \frac{1}{R} \frac{dR}{dV} \right)_{\text{ref. voltage}} 
\]

(Measured in ppm/V)

- If VCR is Constant

\[
R(V_2) = R(V_1) e^{\frac{V_2 - V_1}{10^6} \cdot VCR} \approx R(V_1) \left[ 1 + (V_2 - V_1) \frac{VCR}{10^6} \right]
\]

- Capacitor variations with voltage can be described by the same equation by replacing the resistance with the capacitance
Resistor Nonidealities: Temperature & Voltage

- Temperature and voltage coefficients are often quite large for diffused resistors

- Temperature and voltage coefficients are often quite small for poly and metal resistors

Why do diffused resistors have large Temp. and Voltage coefficients?

- Mobility changes significantly with temperature
- Depletion region thickness with the substrate
Basic Devices

- Resistor
- Diode
- Capacitor
- MOSFET
- BJT
Basic Devices: Diodes (PN Junctions)

- **Silicon Dopants in Semiconductor Processes**

- **Boron (B) →** widely used for creating p-type regions (source and drain of PMOS, p-type substrates)

- **Phosphorus (P) →** diffuses fast → widely used for creating large n-type regions such the bulk of a PMOS

- **Arsenic (As) →** diffuses fast → widely used for creating small n-type regions such the source and drain of NMOS
So what happens when we interface a p-type material with an n-type material??

- Note that a p-type material has too many mobile holes → BUT the total charge is still ZERO because it is balanced by the negative immobile ions in the material.
- Note that a n-type material has too many mobile electrons → BUT the total charge is still ZERO because it is balanced by the positive immobile ions in the material.
So what happens when we interface a p-type material with an n-type material??

Depletion region created that is ionized but void of carriers
So what happens when we interface a p-type material with an n-type material??

If doping levels are identical, depletion region extends equally into n-type and p-type regions.
So what happens when we interface a p-type material with an n-type material??

Extends farther into p-type region if p-doping lower than n-doping
So what happens when we interface a p-type material with an n-type material??

Extends farther into n-type region if n-doping lower than p-doping
Basic Devices: Diodes (PN Junctions)

- If the voltage across the p to n junction is positive → Referred to as “Forward Bias”
- If the voltage across the p to n junction is negative → Referred to as “Reverse Bias”
- As forward bias increases, depletion region thins and current starts to flow and grows very rapidly as the forward bias increases
- Current is very small under reverse bias
Basic Devices: Diodes (PN Junctions)
Diodes (PN Junctions): Ideal Model

- As forward bias increases, depletion region thins and current starts to flow and grows very rapidly as the forward bias increases.
- Current is very small under reverse bias.

This simple model is often referred to as the “Ideal” diode model.
This model means that the diode behaves like a rectifier. It passes current only in one direction but not the other.

**Ideal Diode Model**

- If $I_D > 0$ → *Forward Bias* → Assume $V_D = 0$
- If $V_D < 0$ → *Reverse Bias* → Assume $I_D = 0$

Under Reverse Bias
Under Forward Bias
Diodes (PN Junctions): Applications

◆ A Rectifier

\[ V_{IN} = V_M \sin \omega t \]

Ideal Diode Model

\[ V_{OUT} \]

\[ I_D \]
Diodes (PN Junctions): I-V Characteristics

◆ We need a more realistic model of the diode

\[
I_D = I_S \left( e^{\frac{V_d}{V_t}} - 1 \right)
\]

\(I_S\) in the 10fA to 100fA range

\(V_t = \frac{kT}{q}\) (\(T\) is in Kelvin)

\(k = 1.380 \, 6504(24) \times 10^{-23} \, \text{JK}^{-1}\)

\(k/q = 8.62 \times 10^{-5} \, \text{VK}^{-1}\)

What is \(V_t\) at room temp?

\(V_t\) is about 26mV at room temp

Diode equation due to William Schockley, inventor of BJT

In 1919, William Henry Eccles coined the term **diode**
Diodes (PN Junctions): I-V Characteristics

\[ I_D = I_S \left( e^{\frac{V_d}{V_t}} - 1 \right) \]

The diode equation can be simplified a bit

If \( V_d \ll -V_t \rightarrow \) Reverse Bias \( \rightarrow I_D \approx -I_S \frac{V_d}{V_t} \)

If \( V_d \gg V_t \rightarrow \) Forward Bias \( \rightarrow I_D \approx I_S e^{\frac{V_d}{V_t}} \)
Diodes (PN Junctions): I-V Characteristics

If $V_d \ll -V_t \rightarrow$ Reverse Bias $\rightarrow I_D \approx -I_S \frac{V_d}{V_t}$

If $V_d >> V_t \rightarrow$ Forward Bias $\rightarrow I_D \approx I_S e^{V_t}$

- The simplified diode equation works pretty well EXCEPT when $V_d$ is too close to zero $\rightarrow$ Can we prove that?
- How much error is introduced using the simplification for $V_d > 0.5V$?

$$\epsilon = \frac{I_S \left( e^{V_t} - 1 \right) - I_S e^{V_t}}{I_S \left( e^{V_t} - 1 \right)} < \frac{1}{\frac{0.5}{e^{0.026}}} = 4.4 \times 10^{-9}$$

- How much error is introduced using the simplification for $V_d < -0.5V$?

$$\epsilon < e^{0.026} = 4.4 \times 10^{-9}$$

- The simplification is really worthwhile
Diodes (PN Junctions): I-V Characteristics

- In general, the following model is good enough for most applications

\[ I_D = \begin{cases} 
  I_S e^{nV_t} & V_d > 0 \\
  0 & V_d < 0 
\end{cases} \]

\[ I_D = J_S A e^{nV_t} \]

- \( I_S = J_S \times A \) Saturation Current
- \( J_S = \) Saturation Current Density (in the 1aA/u^2 to 1fA/u^2 range)
- \( A = \) Junction Cross Section Area
- \( V_t = kT/q \) (\( k/q = 8.62 \times 10^{-5} \text{V/°K} \))
- \( n \) is approximately 1
Diodes (PN Junctions): I-V Characteristics

- In general, the following model is good enough for most applications

\[
I_D = \begin{cases} 
    I_S e^{nV_t} = J_S A e^{nV_t} & V_d > 0 \\
    0 & V_d < 0 
\end{cases}
\]

- It is important to note that the saturation current density is a strong function of temperature \(\rightarrow\) Assuming \(n=1\) and forward bias

\[
I_D = \left( J_{SX} \left[ T^m e^{\frac{-V_G}{V_t}} \right] \right) A e^{nV_T}
\]

Typical values for key parameters: \(J_{SX}=0.5A/\mu^2, V_{G0}=1.17V, m=2.3\)
Let’s take an example → What percent change in $I_S$ will occur for a 1°C change in temperature at room temperature?

$$I_D = \left( J_{Sx} \left[ T^{m} e^{-\frac{V_{G0}}{V_t}} \right] \right) Ae^{nV_t}$$

$$\Delta I_S = \left( J_{Sx} \left[ T^{m} e^{-\frac{V_{G0}}{V_t}} \right] \right) A - \left( J_{Sx} \left[ T^{m} e^{-\frac{V_{G0}}{V_t}} \right] \right) A = \left( T^{m} e^{-\frac{V_{G0}}{V_t}} \right) - \left( T^{m} e^{-\frac{V_{G0}}{V_t}} \right)$$

$$\Delta I_S = \left( 1.240 \times 10^{-15} \right) - \left( 1.025 \times 10^{-15} \right) = 21\%$$
**Diodes (PN Junctions): I-V Characteristics**

- In general, the following model is good enough for most applications → How easy is it to use such model in the context of circuits?

- Let’s try an example → Find the output of the following basic circuit

\[
I_D = \begin{cases} 
\frac{V_d}{nV_t} & V_d > 0 \\
0 & V_d < 0 
\end{cases}
\]

\[
I_D = I_S e^{nV_t} = J_S A e^{nV_t}
\]
Diodes (PN Junctions): I-V Characteristics

\[
\begin{align*}
V_{IN} &= V_d + I_D R \\
V_{OUT} &= I_D R \\
I_D &= I_S e^{V_d / V_t} \\
V_{OUT} &= I_S R e^{V_{IN} - V_{OUT} / V_t}
\end{align*}
\]

- Even this very simple circuit, we don’t have a closed-form solution if we use the diode equation.

- This is mainly due to the nonlinear nature of diode.

- We would like to develop a simpler model of the diode without compromising accuracy too much.
Diodes (PN Junctions): Piecewise Linear Model

Let’s study the diode model graphically

![Diode Characteristics graph](image)

\[ I_D = I_S \left( e^{\frac{V_d}{V_t}} - 1 \right) \]

Power Dissipation Becomes Destructive if \( V_d > 0.85V \) (actually even less)
Diodes (PN Junctions): Piecewise Linear Model

- So let’s zoom-in at around 0.6V

\[ I_D = I_S \left( \frac{V_d}{V_t} - 1 \right) \]

- For two decades of current change, \( V_d \) is close to 0.6V
- This is the most useful current range for many applications
Diodes (PN Junctions): Piecewise Linear Model

- A widely used Piecewise Linear Model of the diode

\[ I_D = I_S \left( \frac{V_d}{V_t} - 1 \right) \]

- If \( I_D > 0 \) → Forward Bias → Assume \( V_d = 0.6V \)
- If \( V_d < 0.6V \) → Reverse Bias → Assume \( I_D = 0 \)

Diode Characteristics

![Diode Characteristics Graph](image-url)
Can we do better?

We can approximate the current profile as a straight line.

A straight line relation between current a voltage changes correspond to a resistance → We call it the “ON” resistance of the diode $R_D$

$R_D$ is often small → in the 20Ω to 100Ω range
Diodes (PN Junctions): Piecewise Linear Model

- **Piecewise Linear Model of the diode with the diode resistance**

\[ I_D = I_S \left( \frac{V_d}{V_t} - 1 \right) \]

If \( I_D > 0 \) → **Forward Bias** → Assume \( V_d = 0.6V + I_D R_D \)

If \( V_d < 0.6V \) → **Reverse Bias** → Assume \( I_D = 0 \)
Diodes (PN Junctions): Piecewise Linear Model

- **Piecewise Linear Model of the diode with the diode resistance → Equivalent Circuits**

  If \( I_D > 0 \) → Forward Bias → Assume \( V_d = 0.6V + I_D R_D \)

  If \( V_d < 0.6V \) → Reverse Bias → Assume \( I_D = 0 \)
**Diodes (PN Junctions): Model Summary**

**Diode Equation**

\[
I_D = I_S \left( e^{\frac{V_d}{V_t}} - 1 \right)
\]

**Piecewise Linear Models**

\[
\begin{align*}
I_D &= 0 & \text{If } V_d &< 0.6V \\
V_d &= 0.6V & \text{If } I_D &> 0
\end{align*}
\]

\[
\begin{align*}
I_D &= 0 & \text{If } V_d &< 0.6V \\
V_d &= 0.6V + I_D R_D & \text{If } I_D &> 0
\end{align*}
\]

\[
\begin{align*}
I_D &= 0 & \text{If } V_d &\leq 0 \\
V_d &= 0 & \text{If } I_D &> 0
\end{align*}
\]

Ideal
Diodes (PN Junctions): Using Models

- Too many models → which should be used? → the simplest that will give acceptable results

- When are piecewise linear models adequate?
  - When it doesn’t make much difference whether $V_d=0.6V$ or $V_d=0.7V$

- When is the ideal piecewise linear model adequate?
  - When it doesn’t make much difference whether $V_d=0V$ or $V_d=0.7V$
Diodes (PN Junctions): Using Models

◆ How to use Piecewise Linear Models for Nonlinear Devices when Analyzing Electronic Circuits?

◆ The Sequence
  ➢ Make an “educated” guess of the state of the device (on, off, etc.)
  ➢ Analyze the corresponding linear circuit
  ➢ Verify if the state assumption is indeed valid
  ➢ Repeat steps the previous steps if verification fails

◆ Things to observe
  ➢ Analysis is generally simplified dramatically
  ➢ Approach is applicable to a wide variety of nonlinear devices
  ➢ Closed-form solutions give insight into performance of circuit
  ➢ Usually much faster than solving the nonlinear circuit directly
  ➢ Wrong guesses in the state of the device do not compromise solution → verification will fail
  ➢ Helps to Guess SMART the first time
Diodes (PN Junctions): Example 1

- **Example → Determine** $I_{OUT}$ **for the following circuit**

- **Solution Strategy**
  - Assume PWL model with $V_d=0.6V$, $R_D=0$
  - Guess state of diode (Come on, IT IS ON)
  - Analyze circuit with model
  - Validate state of guess
  - Assume PWL with $V_d=0.7V$
  - Guess state of diode (ON)
  - Analyze circuit with model
  - Validate state of guess
  - Show difference between results using these two models is indeed small
  - If difference is not small, must use a different model
Diodes (PN Junctions): Example 1

- Assume PWL model with $V_d=0.6V$, $R_D=0$
- Guess state of diode (ON)
- Analyze circuit with model

\[
I_{OUT} = \frac{12V - 0.6V}{10K} = 1.14mA
\]

- Validate state of guess $\rightarrow$ If the diode is indeed on, then $I_D$ must be $>0$

\[
I_D = I_{OUT} = 1.14mA > 0
\]
Diodes (PN Junctions): Example 1

- Assume PWL model with $V_d=0.7V$, $R_D=0$
- Guess state of diode (ON)
- Analyze circuit with model

$$I_{OUT} = \frac{12V - 0.7V}{10K} = 1.13mA$$

- Validate state of guess $\rightarrow$ If the diode is indeed on, then $I_D$ must be $>0$

$$I_D = I_{OUT} = 1.13mA > 0$$
Diodes (PN Junctions): Example 1

- Show that the difference between the results using these two models is small

\[ I_{\text{OUT}} = 1.14 \text{mA} \text{ and } I_{\text{OUT}} = 1.13 \text{ mA} \]

- The are very close → It is ok to conclude that \( I_{\text{OUT}} = 1.14 \text{mA} \)
Diodes (PN Junctions): Example 2

Example → Determine $I_{\text{OUT}}$ for the following circuit

Solution Strategy
- Assume PWL model with $V_d=0.6\,\text{V}$, $R_D=0$
- Guess state of diode (Come on, IT IS ON)
- Analyze circuit with model
- Validate state of guess
- Assume PWL with $V_d=0.7\,\text{V}$
- Guess state of diode (ON)
- Analyze circuit with model
- Validate state of guess
- Show difference between results using these two models is indeed small
- If difference is not small, must use a different model
Diodes (PN Junctions): Example 2

- Assume PWL model with $V_d=0.6V$, $R_D=0$
- Guess state of diode (ON)
- Analyze circuit with model

\[ I_{OUT} = \frac{0.8V-0.6V}{10K} = 20\mu A \]

- Validate state of guess → If the diode is indeed on, then $I_D$ must be $>0$

\[ I_D = I_{OUT} = 20\mu A > 0 \]
Diodes (PN Junctions): Example 2

- Assume PWL model with $V_d=0.7V$, $R_D=0$
- Guess state of diode (ON)
- Analyze circuit with model

\[ I_{OUT} = \frac{0.8V - 0.7V}{10K} = 10 \mu A \]

- Validate state of guess $\rightarrow$ If the diode is indeed on, then $I_D$ must be $>0$

\[ I_D = I_{OUT} = 10 \mu A > 0 \]
Diodes (PN Junctions): Example 2

Show that the difference between the results using these two models is small

\[ I_{\text{OUT}} = 10\mu A \text{ and } I_{\text{OUT}} = 20\mu A \]

That is NOT CLOSE AT ALL \(\rightarrow\) what do we do??

We must use the diode equation!

\[ I_{\text{OUT}} = \frac{0.8 - V_d}{10K} \quad I_{\text{OUT}} = I_S e^{\frac{V_d}{V_t}} \]

Solve simultaneously, assume \(V_t = 25\text{mV}\), \(I_S = 1\text{fA}\)

Solving these two equations by iteration, obtain \(V_d = 0.6148\text{V}\) and \(I_{\text{OUT}} = 18.60\mu A\)
Diodes (PN Junctions): Comparison

- Do I have to go through all this just to figure out that I have to use the diode equation??
- Not necessarily → If by observing the voltage levels in your circuit you realize that they are too close to 0.6V, then very likely you will have to use the diode model
- Compare the two examples
Diodes (PN Junctions): Types

◆ There are many types of diodes (PN Junctions)

- Signal or Rectifier
- Pin or Photo
- Light Emitting LED
- Laser Diode
- Zener
- Varactor or Varicap

◆ Metal-semiconductor junction diodes

- Schottky Barrier
Basic Devices

- Resistor
- Diode
- Capacitor
- MOSFET
- BJT
Basic Devices: Capacitors

- There are several types of capacitors in semiconductor processes
  - Parallel Plate
  - Fringe
  - Junction
Capacitors: Parallel Plate

- Parallel plate capacitors are formed through the overlap between two vertically spaced conductive plates with an insulator in between → Two different layers of material are needed
- The top plate is typically smaller in area than the bottom
- Capacitance is determined by the intersection area

\[ C = \frac{\varepsilon A}{d} \]

A = area of intersection of \( A_1 \) & \( A_2 \)
Capacitors: Parallel Plate

◆ The total capacitance can be expressed in terms of capacitance per unit area

\[ C = \left( \frac{\varepsilon}{d} \right) \times A \]

Define \( C_d = \frac{\varepsilon}{d} \) \[ \rightarrow \quad C = C_d \times A \]

◆ The capacitance may or may not be linear (not voltage dependent) depending on which layers are used
  ➢ Metal-to-Metal and Poly-to-Poly are very linear
  ➢ Poly-to-Silicon is not
Capacitors: Fringe

- Fringe capacitors are formed through the overlap between two horizontally spaced conductive plates with an insulator in between → only a single layer of material is needed
- Typically implemented in Metal or Poly Layers → Very linear

\[ C = \frac{\epsilon A}{d} \]

\( A = \text{area of intersection} \)
The problem with fringe capacitors is that thickness of layers is typically very small → the overlap area is very small → capacitance per unit area is very small.

We often have to increase the area through fork structures.
Capacitors: Junction

- This type of capacitance is formed across the depletion region of PN junctions
  - $d$ is voltage dependent $\rightarrow$ Junction capacitors are very nonlinear
  - Usually considered an undesired parasitic capacitance, but have some useful applications such as varactors (voltage controlled capacitors) $\rightarrow$ Common in early radios for channel tuning

\[ C = \frac{\varepsilon A}{d} \]

\[ C = \frac{C_{jo}A}{\left(1 - \frac{V_D}{\varphi_B}\right)^n} \quad \text{for} \quad V_{FB} < \frac{\varphi_B}{2} \]
The nonlinearity of junction capacitors is actually substantial.

\[
C = \frac{C_{j0}A}{(1 - \frac{V_D}{\phi_B})^n}
\]

for \( V_{FB} < \frac{\phi_B}{2} \)

\( \phi_B \approx 0.6 \text{V} \quad n \approx 0.5 \)
Basic Devices

- Resistor
- Diode
- Capacitor
- MOSFET
- BJT
The MOSFET is a 4-terminal device. We will start by considering the 4th terminal (the bulk) always connected to the source to develop a model, then the impact of the 4th terminal (the bulk) will be appended to the model later.

Let’s start with the n-channel MOSFET.
N-Channel MOSFET
Depletion region is always created whenever there is an interface between an n-type and a p-type material.
Apply a very small $V_{GS}$ (assume $V_{DS}$ very small and $V_{BS} = 0$) → depletion region continues to develop underneath the gate, but the device is off → no current flow from drain to source → This region of operation is called the “cutoff” region.

\[ V_{DS} \]
\[ V_{GS} \]
\[ V_{BS} \]
\[ I_{D} \]
\[ I_{G} \]
\[ I_{B} \]

\[ I_{D}=0 \]
\[ I_{G}=0 \]
\[ I_{B}=0 \]
As you increase $V_{GS}$ (assume $V_{DS}$ very small and $V_{BS} = 0$) → depletion region underneath the gate continues to grow but the device continues to be off → Still in the “cutoff” region.
As you further increase $V_{GS}$ (assume $V_{DS}$ very small and $V_{BS}=0$) → the area underneath the gate starts to be inverted → It becomes an n-type layer

- The value of $V_{GS}$ at which inversion takes place is call the threshold voltage ($V_T$)
- Current flows between the drain and the source and the device behaves like a thin film resistor → This region of operation is called the “triode” or “linear” or “ohmic” region

\[
\begin{align*}
V_{GS} & \quad \text{(V DS very small and V BS =0)} \\
V_{DS} & \\
V_{BS} & \\
I_B & \\
I_G & \\
I_D &= V_{DS} \\
I_G &= 0 \\
I_B &= 0
\end{align*}
\]
N-Channel MOSFET: Triode Region

- With $V_{DS}$ very small $\rightarrow$ The device behaves like a resistor between the drain and the source.
- The resistance will strongly depend on $V_{GS}$ and the transistor size.
- Larger $V_{GS}$ $\rightarrow$ deeper inversion layer $\rightarrow$ less channel resistance.
- Wider transistor $\rightarrow$ wider channel $\rightarrow$ less channel resistance.
- Longer transistor $\rightarrow$ longer channel $\rightarrow$ more channel resistance.

For $V_{DS}$ small

- $I_D = \mu C_{OX} \frac{W}{L} (V_{GS} - V_T) V_{DS}$
- $I_G = I_B = 0$

$R_{CH} = \frac{L}{W} \frac{1}{\mu C_{OX} (V_{GS} - V_T)}$

$\mu$ $\rightarrow$ Electron Mobility
$C_{OX}$ $\rightarrow$ Gate Capacitance per unit area
N-Channel MOSFET: Triode Region

Since the channel resistance is controlled by $V_{GS}$, it is termed a Voltage Controlled Resistance (VCR).

For $V_{DS}$ small

$$R_{CH} = \frac{L}{W} \mu C_{OX} \frac{1}{(V_{GS} - V_T)}$$
What happens when we now start increasing $V_{DS}$?

The channel starts to become thinner towards the drain side $\to$ So channel resistance becomes different $\to$ Nonlinear behavior $\to$ The drain current starts to become nonlinear with respect to $V_{DS}$

Yet, we continue to call this region of operation “triode” or “linear” or “ohmic”

(N-Channel MOSFET: Triode Region)
N-Channel MOSFET: Triode Region

We now must take into account the nonlinearity in the channel resistance and drain current.

For small $V_{DS}$

$$I_D = \mu C_{ox} \frac{W}{L} (V_{GS} - V_T) V_{DS}$$

$$R_{CH} = \frac{L}{W} \frac{1}{\mu C_{ox} (V_{GS} - V_T)}$$

$I_G = I_B = 0$

For $V_{DS}$ larger

$$I_D = \mu C_{ox} \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS}$$

$I_G = I_B = 0$
N-Channel MOSFET: Saturation Region

- If we further increase $V_{GS}$, the inversion layer disappears at the drain side.
- The critical values at which this happens is $V_{DS} = V_{GS} - V_T$.
- Increasing $V_{DS}$ beyond that critical value no longer changes the channel; the drain current stops increasing with $V_{DS}$.
- This region of operation is called the “saturation” region.

$$V_{BS} = 0$$

$V_{DS}$

$V_{GS}$

$V_{BS}$

$I_D$?

$I_G = 0$

$I_B = 0$

Increase $V_{DS}$ even more
The drain current gets stuck at its value when \( V_{DS} = V_{GS} - V_T \) regardless of what the actual \( V_{DS} \) is (as long as it is larger than the critical value of \( V_{GS} - V_T \)).

\[
I_D = \mu C_{OX} \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} \quad \text{in triode region}
\]

Since the voltage across the channel gets stuck at \( V_{GS} - V_T \), then:

\[
I_D = \mu C_{OX} \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{GS} - V_T}{2} \right)(V_{GS} - V_T)
\]

or equivalently \( I_D = \frac{\mu C_{OX} W}{2L} (V_{GS} - V_T)^2 \).
N-Channel MOSFET: Saturation Region

- With $V_{DS} > (V_{GS} - V_T)$ → The device behaves like a current source between the drain and the source
- The value of the current will strongly depend on $V_{GS}$ and the transistor size
- Larger $V_{GS}$ → deeper inversion layer → larger current
- Wider transistor → wider channel → larger current
- Longer transistor → longer channel → less current

For $V_{DS} > V_{GS} - V_T$

\[ I_D = \mu C_{OX} \frac{W}{2L} (V_{GS} - V_T)^2 \]

$I_G = I_B = 0$
N-Channel MOSFET: Saturation Region

- Since the current is controlled by $V_{GS}$, it is termed a Voltage Controlled Current Source (VCCS)

For $V_{DS} > V_{GS} - V_T$

\[ I_D = \mu C_{OX} \frac{W}{2L} (V_{GS} - V_T)^2 \]
N-Channel MOSFET: Model Summary

- This is the third model we introduced for the MOSFET $\rightarrow$
  It is termed the Ideal Square-Law model of the transistor

$$I_D = \begin{cases} 
0 \\ 
\mu C_{OX} \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} \\
\mu C_{OX} \frac{W}{2L} \left( V_{GS} - V_T \right)^2 
\end{cases}$$

$$V_{GS} \leq V_T$$

Cutoff

$$V_{GS} \geq V_T \), \hspace{0.1cm} V_{DS} < \hspace{0.1cm} V_{GS} - V_T$$

Triode

$$V_{GS} \geq V_T \), \hspace{0.1cm} V_{DS} \geq \hspace{0.1cm} V_{GS} - V_T$$

Saturation

- Deep triode is a special case of the triode operation when $V_{DS} \ll V_{GS} - V_T$
- In this case the transistor is modeled as a resistor

$$I_D \approx \mu C_{OX} \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} \Rightarrow R_{CH} = \frac{L}{W \mu C_{OX} \left( V_{GS} - V_T \right)} \frac{1}{V_{GS} - V_T}$$
N-Channel MOSFET: Model Summary

What does the above model of the transistor mean exactly?

1. The transistor behaves like an open circuit between the drain and the source in the cutoff region

2. The transistor behaves like a nonlinear (depends of $V_{DS}$) VCR between the drain and the source in the triode region → in deep triode, the resistance can be assumed linear (independent of $V_{DS}$)

3. The transistor behaves like an ideal VCCS between the drain and the source in the saturation region (independent of $V_{DS}$)

4. The value of the resistance in the triode region, and the value of the current source in the saturation region are determined by $V_{GS}$ and transistor size

\[
I_D = \begin{cases} 
0 & V_{GS} \leq V_T \\
\mu C_{OX} \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} & V_{GS} \geq V_T, V_{DS} < V_{GS} - V_T \\
\mu C_{OX} \frac{W}{2L} (V_{GS} - V_T)^2 & V_{GS} \geq V_T, V_{DS} \geq V_{GS} - V_T 
\end{cases}
\]

$V_{BS} = 0$

$V_G = I_D = I_B = 0$
N-Channel MOSFET: Model Summary

This is a nonlinear model characterized by the functions $f_1$, $f_2$, and $f_3$ where we have assumed that the port voltages $V_{GS}$ and $V_{DS}$ are the independent variables and the terminal currents are the dependent variables.

\[
I_D = \begin{cases} 
0 & V_{GS} \leq V_T \\
\mu C_{OX} \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} & V_{GS} \geq V_T, \ V_{DS} < V_{GS} - V_T \\
\mu C_{OX} \frac{W}{2L} \left( V_{GS} - V_T \right)^2 & V_{GS} \geq V_T, \ V_{DS} \geq V_{GS} - V_T \\
\end{cases}
\]

$I_G = I_B = 0$

\[
\begin{align*}
I_D &= f_1 \left( V_{GS}, V_{DS} \right) \\
I_G &= f_2 \left( V_{GS}, V_{DS} \right) \\
I_B &= f_3 \left( V_{GS}, V_{DS} \right)
\end{align*}
\]
The operation the n-channel MOSFET can be described graphically in all regions.

At the border between triode and saturation:

\[ V_{DS} = V_{GS} - V_T \rightarrow I_D = \mu C_{ox} \frac{W}{2L} V_{DS}^2 \]

\[ I_D = \begin{cases} 
0 & V_{GS} \leq V_T \\
\mu C_{ox} \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} & V_{GS} > V_T, V_{DS} < V_{GS} - V_T \\
\mu C_{ox} \frac{W}{2L} \left( V_{GS} - V_T \right)^2 & V_{GS} > V_T, V_{DS} \geq V_{GS} - V_T \\
I_G = I_B = 0 & \end{cases} \]
Since the knowing the operation region is required in order to pick the corresponding equation model, we have to follow the same strategy used in solving problems with diodes

- Make an educated guess about which region of operation the transistor is in
- Analyze circuit with the corresponding model
- Validate if the guess is valid
- If the guess was not valid, then redo with a different guess
N-Channel MOSFET: Example

- Determine the output voltage for the following circuit using the Ideal Square-Law model of the MOSFET. Assume $V_T=1V$ and $\mu C_{OX}=100\mu AV^{-2}$

Since $V_{GS}>V_T$, an educated guess would be that $M_1$ is operating in either saturation or triode region

- Since $V_{GS}>V_T$, an educated guess would be that $M_1$ is operating in either saturation or triode region
N-Channel MOSFET: Example

Let’s guess that $M_1$ is in saturation

\[
I_D = \begin{cases} 
0 & \text{if } V_{GS} \leq V_T \\
\mu C_{ox} \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} & \text{if } V_{GS} \geq V_T, V_{DS} < V_{GS} - V_T \\
\mu C_{ox} \frac{W}{2L} \left( V_{GS} - V_T \right)^2 & \text{if } V_{GS} \geq V_T, V_{DS} \geq V_{GS} - V_T
\end{cases}
\]

Required verification: $V_{DS} > V_{GS} - V_T$

\[
5V = I_D 10K + V_{OUT}
\]

\[
I_D = \frac{\mu C_{ox} W}{2L} (3 - V_T)^2
\]

Can eliminate $I_D$ between these 2 equations to obtain $V_{OUT}$
Let’s guess that $M_1$ is in saturation

\[
5V = I_D 10K + V_{OUT}
\]

\[
I_D = \frac{\mu C_{OX} W}{2L} (3-V_T)^2
\]

Required verification: $V_{DS} > V_{GS} - V_T$

\[
V_{OUT} = 5V - 10K \left[ \frac{100 \mu A V^{-2} 2\mu}{2 \cdot 2\mu} (2V)^2 \right]
\]

\[
V_{OUT} = 5V - 10K \left[ \frac{100 \mu A V^{-2} 2\mu}{2 \cdot 2\mu} (2V)^2 \right]
\]

\[
V_{OUT} = -5V
\]

Verification: $V_{DS} = V_{OUT}$

$-5 > (3V - 1V) \rightarrow \text{No!}$ So verification fails and Guess of region is invalid
N-Channel MOSFET: Example

Let's guess that $M_1$ is in triode

$$I_D = \begin{cases} 
0 & V_{GS} \leq V_T \\
\frac{W}{L} \mu C_{ox} (V_{GS} - V_T - \frac{V_{DS}}{2}) V_{DS} & V_{GS} > V_T, V_{DS} < V_{GS} - V_T \\
\frac{W}{2L} \mu C_{ox} (V_{GS} - V_T)^2 & V_{GS} > V_T, V_{DS} \geq V_{GS} - V_T 
\end{cases}$$

$$5V = I_D 10K + V_{OUT}$$

$$I_D = \frac{\mu C_{ox} W}{L} \left(3-V_T - \frac{V_{OUT}}{2}\right) V_{OUT}$$

Required verification: $V_{DS} < V_{GS} - V_T$
Let’s guess that $M_1$ is in triode

\[ 5V = I_D 10K + V_{OUT} \]

\[ I_D = \frac{\mu C_{OX} W}{L} \left( 3 - V_T - \frac{V_{OUT}}{2} \right) V_{OUT} \]

Required verification: $V_{DS} < V_{GS} - V_T$

\[ V_{OUT} = 5V - 10K \left[ \frac{100\mu A V^{-2} 10\mu}{2\mu} \left( 2V - \frac{V_{OUT}}{2} \right) V_{OUT} \right] \]

\[ V_{OUT} = 0.515V \]

Verification: $V_{DS} = V_{OUT}$

\[ 0.515 < (3V-2V) \text{ Yes! So verification succeeds and triode region is valid} \]
So far we have developed 3 different models for the operation of the MOSFET:

- **Ideal Switch-Level Model** → Simple Ideal ON/OFF view → Models the ideal operation in triode and cutoff regions.

- **Switch-Level Model with channel resistance** → Simple ON/OFF view → Models realistic operation in deep triode region and ideal operation in cutoff region.

- **Ideal Square-Law Model** → Models realistic operation in triode, cutoff, and saturation regions.

There are still more complicated models to describe further nonidealities in the operation of the MOSFET.
N-channel MOSFET Model Extension: Channel Length Modulation

- In saturation region, the MOSFET is not really an ideal VCCS that is independent of $V_{DS}$
- If we further increase $V_{GS}$, the inversion layer disappears at the drain side
- The critical values at which this happens: $V_{DS}=V_{GS}-V_T$
- Increasing $V_{DS}$ beyond the critical value DOES CHANGE the channel just a little bit. This is called channel length modulation. The drain current will slightly increase with $V_{DS}$
N-channel MOSFET Model Extension: Channel Length Modulation

- Projections intersect $-V_{DS}$ axis at same point, termed Early Voltage
- Typical values from 20V to 200V
- Usually use parameter $\lambda$ instead of $V_A$ in MOS model
N-channel MOSFET Model Extension: Channel Length Modulation

\[ I_D = \begin{cases} 
0 & V_{GS} \leq V_T \\
\mu C_{OX} \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} & V_{GS} \geq V_T, V_{DS} < V_{GS} - V_T \\
\mu C_{OX} \frac{W}{2L} \left( V_{GS} - V_T \right)^2 \times \left( 1 + \lambda V_{DS} \right) & V_{GS} \geq V_T, V_{DS} \geq V_{GS} - V_T
\end{cases} \]

\[ I_G = I_B = 0 \]

Note: This introduces small discontinuity (not shown) in model at SAT/Triode transition
N-channel MOSFET Model Extension: Channel Length Modulation

With $V_{DS} > (V_{GS} - V_T)$ → The device behaves like a nonideal VCCS between the drain and the source → This nonideality is modeled as a resistance in parallel with the VCCS → Termed the output resistance of the transistor

\[ I_D = \mu C_{OX} \frac{W}{2L} (V_{GS} - V_T)^2 \times (1 + \lambda V_{DS}) \]

\[ = \mu C_{OX} \frac{W}{2L} (V_{GS} - V_T)^2 + \lambda \mu C_{OX} \frac{W}{2L} (V_{GS} - V_T)^2 V_{DS} \]

\[ = I_{DEQ} + \left( \frac{V_{DS}}{R_{DEQ}} \right) \]

For $V_{DS} > V_{GS} - V_T$

\[ I_{DEQ} = \mu C_{OX} \frac{W}{2L} (V_{GS} - V_T)^2 \]

\[ R_{DEQ} = \frac{1}{\lambda \mu C_{OX} \frac{W}{2L} (V_{GS} - V_T)^2} = \frac{1}{\lambda I_{DEQ}} \approx \frac{1}{\lambda I_D} \]
The transistor is a 4-terminal device. So far we assumed that the bulk is connected to the source $V_{BS} = 0$.

What if it is not $V_{BS}$? It will change the depletion region thickness, change the thickness of the channel, and can be modeled as a change in the threshold voltage $V_T$.

- Positive $V_{BS}$: Channel becomes thicker $\rightarrow V_T$ becomes lower.
- Negative $V_{BS}$: Channel becomes thinner $\rightarrow V_T$ becomes higher.

$V_{BS} > 0$ is ok as long as it is less than 0.6V $\rightarrow$ otherwise the bulk source diode will turn on and may destroy the device. We generally always keep $V_{BS} < 0$ but prefer $V_{BS} = 0$.

$$V_T = V_{T0} + \gamma \left( \sqrt{\phi - V_{BS}} - \sqrt{\phi} \right)$$
N-Channel MOSFET Model Extension: Bulk Voltage

- Change in VT with VBS can be substantial

\[ \gamma \approx 0.4V^{1/2} \]

\[ V_T = V_{T0} + \gamma \left( \sqrt{\phi - V_{BS}} - \sqrt{\phi} \right) \]

\[ \phi \approx 0.6V \]
Change in VT with VBS can be substantial

\[ \gamma \approx 0.4V^{\frac{1}{2}} \]

\[ \phi \approx 0.6V \]

\[ V_T = V_{T0} + \gamma\left(\sqrt{\phi - V_{BS}} - \sqrt{\phi}\right) \]

\[ \Delta V = ? \]

\[ \Delta V_T = V_T - V_{T0} = \gamma\left(\sqrt{\phi - V_{BS}} - \sqrt{\phi}\right) \]

\[ \Delta V_T \approx 0.4\left(\sqrt{0.6 - -5} - \sqrt{0.6}\right) = 0.64V \]
**N-Channel MOSFET Model Extension: Summary**

- This is the fourth model we introduced for the MOSFET → It is termed the Extended Square-Law model of the transistor

- **Model Parameters:** \[ \{\mu, C_{OX}, V_{T0}, \gamma, \varphi, \lambda\} \] → Either determined by physics or process technology

- **Design Parameters:** \{W, L, and voltage levels\} → in your hands as a designer

\[
I_D = \begin{cases} 
0 & \text{if } V_{GS} \leq V_T \\
\mu C_{OX} \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} & \text{if } V_{GS} \geq V_T, \ V_{DS} < V_{GS} - V_T \\
\mu C_{OX} \frac{W}{2L} (V_{GS} - V_T)^2 \times (1 + \lambda V_{DS}) & \text{if } V_{GS} \geq V_T, \ V_{DS} \geq V_{GS} - V_T \\
V_T = V_{T0} + \gamma \left( \sqrt{\varphi - V_{BS}} - \sqrt{\varphi} \right) & \text{if } V_{GS} \leq V_T \\
I_G = I_B = 0 & \text{if } V_{GS} \leq V_T
\]

\[
V_{GS} \leq V_T \\
V_{GS} \geq V_T, \ V_{DS} < V_{GS} - V_T \\
V_{GS} \geq V_T, \ V_{DS} \geq V_{GS} - V_T \\
V_T = V_{T0} + \gamma \left( \sqrt{\varphi - V_{BS}} - \sqrt{\varphi} \right) \\
I_G = I_B = 0
\]
So far we have developed 4 different models for the operation of the MOSFET

- Ideal Switch-Level Model → Simple Ideal ON/OFF view → Models the ideal operation in triode and cutoff regions

- Switch-Level Model with channel resistance → Simple ON/OFF view → Models realistic operation in deep triode region and ideal operation in cutoff region

- Square-Law Model → Models realistic operation in triode, cutoff, and saturation regions

- Extended Square-Law Model → Adds channel length modulation and bulk voltage effects to the Ideal Square-Law model

There are still more complicated models to describe further nonidealities in the operation of the MOSFET
N-Channel MOSFET: Short Devices

- As the length of the transistor becomes very short, the electric field across the channel becomes large if the voltage levels stay the same.
- Around 2V/μ electric field → Velocity saturation occurs and the behavior of the transistor deviates from the Extended Square-Law model.
- The model used to describe this case is termed the α-Power model.

\[
I_D = \begin{cases} 
0 & V_{GS} \leq V_T \\
\frac{\theta_2}{\theta_1} \mu C_{ox} \frac{W}{L} (V_{GS} - V_T)^\alpha V_{DS} & V_{GS} \geq V_T, \quad V_{DS} < \theta_1 (V_{GS} - V_T)^\frac{\alpha}{2} \\
\theta_2 \mu C_{ox} \frac{W}{L} (V_{GS} - V_T)^\alpha \times (1 + \lambda V_{DS}) & V_{GS} \geq V_T, \quad V_{DS} \geq \theta_1 (V_{GS} - V_T)^\frac{\alpha}{2} \\
V_T = V_{T0} + \gamma \left( \sqrt{\varphi - V_{BS}} - \sqrt{\varphi} \right) & \\
I_G = I_B = 0
\end{cases}
\]
N-Channel MOSFET: Short Devices

- $\alpha$ is termed the velocity saturation index, $2 \geq \alpha \geq 1$
- For long channel devices, $\alpha = 2 \rightarrow$ back to the Extended Square-Law model
- the $\alpha$-Power model is no longer a square law
- Degradation due to velocity saturation is not a desired behavior

\[
I_D = \begin{cases} 
0 & V_{GS} \leq V_T \\
\frac{\theta_2}{\theta_1} \mu C_{ox} \frac{W}{L} (V_{GS} - V_T)^\alpha V_{DS} & V_{GS} \geq V_T, V_{DS} < \theta_1 (V_{GS} - V_T)^\alpha \\
\theta_2 \mu C_{ox} \frac{W}{L} (V_{GS} - V_T)^\alpha \times (1 + \lambda V_{DS}) & V_{GS} \geq V_T, V_{DS} \geq \theta_1 (V_{GS} - V_T)^\alpha \\
V_T = V_{T0} + \gamma (\sqrt{\varphi} - \sqrt{V_{BS} - \sqrt{\varphi}}) & \\
I_G = I_B = 0
\end{cases}
\]
So far we have developed 5 different models for the operation of the MOSFET → These models are all “ANALYTICAL” models good for initial hand calculations

- Ideal Switch-Level Model → Simple Ideal ON/OFF view → Models the ideal operation in triode and cutoff regions
- Switch-Level Model with channel resistance → Simple ON/OFF view → Models realistic operation in deep triode region and ideal operation in cutoff region
- Square-Law Model → Models realistic operation in triode, cutoff, and saturation regions
- Extended Square-Law Model → Adds channel length modulation and bulk voltage effects to the Ideal Square-Law model
- $\alpha$-Power Model → Models realistic operation in triode, cutoff, and saturation regions for short channel devices (may or may not include channel length modulation and bulk voltage effects)

The transistor is still far more complicated than these models → We need more accurate “SIMULATION” models
Berkeley Short-channel IGFET Model (BSIM) are standard simulation models developed by UC Berkeley.

They have evolved over the years and there are many versions of them (BSIM, BSIM2, BSIM3, BSIM4).

They are too complicated and contain a large number of parameters → Need a simulator such as SPICE, SPECTRE, etc.....
N-Channel MOSFET: BSIM Simulation Model

```plaintext
.MODEL CMOSN NMOS ( 
+VERSION = 3.1
+XJ = 1.5E-7
+K1 = 0.8976376
+K3B = -8.2369696
+DVT0W = 0
+DVT0 = 2.7123969
+U0 = 451.2322004
+UC = 1.22401E-11
+AGS = 0.130484
+KETA = -3.043349E-3
+RDSW = 1.367055E3
+WR = 1
+XL = 1E-7
+DWB = 3.676235E-8
+CIT = 0
+CDSCB = 0
+DSUB = 0.0764123
+PDIBLC2 = 2.366707E-3
+PSCB1E0 = 6.611774E8
+PRT = 0
+KTHIL = 0
+UB1 = -7.61E-18
+WL = 0
+WWN = 1
+LLN = 1
+LWL = 0
+CGDO = 2.32E-10
+CG = 4.282017E-4
+CJSW = 3.034055E-10
+CJSWG = 1.64E-10
+CF = 0
+PK2 = -0.0289036

TNOM = 27
NCH = 1.7E17
K2 = -0.09255
W0 = 1.041146E-8
DVT1W = 0
DVTS = 0.4232931
UA = 3.091785E-13
VSAT = 1.715884E5
B0 = 2.446405E-6
A1 = 8.18159E-7
PRWG = 0.0328586
WINT = 2.443677E-7
B1 = 5E-6
VOFF = -1.493503E-4
CDSC = 2.4E-4
ETA0 = 2.342963E-3
PCLM = 2.5941582
CDSDC = 0
PDIBLCB = -0.0431505
DROUT = 0.9919348
PSCBE2 = 3.238266E-4
PVAG = 0
UTE = -1.5
WT = 0.022
UC1 = -5.6E-11
WL = 1
WWL = 0
LW = 0
LWN = 1
CAPMOD = 2
CGSO = 2.32E-10
PB = 0.9317787
PBSW = 0.8
PBSWG = 0.8
FVTH0 = 0.0520855
PKETA = -0.0237483
LEVEL = 49
TOX = 1.42E-8
VTH0 = 0.629035
K3 = 24.0984767
NLX = 1E-9
DVT2W = 0
DVT2 = -0.1403765
UB = 1.702517E-18
A0 = 0.6580918
B1 = 5E-6
NFACOR = 1.0354201
CDSDC = 0
ETAB = -1.5324E-4
PDIBLC1 = 0.8187825
DROUT = 0.9919348
PVAG = 0
WT = 0.022
UAI = 4.31E-9
AT = 3.3E4
WW = 0
LL = 0
LWN = 1
XPART = 0.5
CGBO = 1E-9
MJ = 0.4495867
MJSW = 0.1713852
MJSWG = 0.1713852
PRDSW = 112.8875816
LKETA = 1.728324E-3
)
```
Semiconductor technologies have variations → Usually described in terms of corners → Typical (Nominal) corner, Fast (Strong) corner, and Slow (Weak) corner

Corner models are needed → each corner has different BSIM model parameters values

Different devices may not necessarily be correlated → the combinations may lead to a large number of models

Corner models help covering all possibilities
N-Channel MOSFET: BSIM Simulation Model

- BSIM models are supposed to be scalable $\rightarrow$ means that their parameters are not a function of the transistor size
N-Channel MOSFET: BSIM Simulation Model

- In many advanced technologies, using the same BSIM model for all transistor sizes can yield inaccurate results
- Binning of BSIM models maybe needed → different parameters values per a range of transistor sizes

With 32 bins, this model has 3040 model parameters just for one process corner.

With 5 process corner combination is becomes 15,200 parameters.
N-Channel MOSFET: The State of The Models

- So far we have developed 5 different models for the operation of the MOSFET → These models are all “ANALYTICAL” models good for initial hand calculations
  - Ideal Switch-Level Model → Simple Ideal ON/OFF view → Models the ideal operation in triode and cutoff regions
  - Switch-Level Model with channel resistance → Simple ON/OFF view → Models realistic operation in deep triode region and ideal operation in cutoff region
  - Square-Law Model → Models realistic operation in triode, cutoff, and saturation regions
  - Extended Square-Law Model → Adds channel length modulation and bulk voltage effects to the Ideal Square-Law model
  - $\alpha$-Power Model → Models realistic operation in triode, cutoff, and saturation regions for short channel devices (may or may not include channel length modulation and bulk voltage effects)

- We also discussed BSIM “SIMULATION” models, which include corner models and binning
N-Channel MOSFET: Operating Modes and their Applications

- Most analog circuits operate in saturation region, but can also use triode and cutoff regions
- Digital circuits use the cutoff and deep triode regions

Diagram showing the regions of operation for MOSFETs with axes labeled $I_D$ and $V_{DS}$.
The PMOS transistor operates the same way we described for the NMOS and uses the same models EXCEPT with negative terminal currents, voltages, and threshold voltage.

There are several ways you can deal with the PMOS device.
P-Channel MOSFET: Operation & Model

- You can use the same NMOS model but with negative $V_{GS}$, $V_{DS}$, $V_{BS}$, $I_D$, and $V_{TP}$
- All conditions for operation regions will be flipped

\[
I_D = \begin{cases} 
0 & V_{GS} \geq V_{TP} \\
-\mu_p C_{OX} \frac{W}{L} \left( V_{GS} - V_{TP} - \frac{V_{DS}}{2} \right) V_{DS} & V_{GS} \leq V_{TP}, V_{DS} > V_{GS} - V_{TP} \\
-\mu_p C_{OX} \frac{W}{2L} \left( V_{GS} - V_{TP} \right)^2 \times \left( 1 - \lambda V_{DS} \right) & V_{GS} \leq V_{TP}, V_{DS} \leq V_{GS} - V_{TP} \\
V_{TP} = V_{TP0} - \gamma \left( \sqrt{\phi + V_{BS}} - \sqrt{\phi} \right) & 
\end{cases}
\]

$I_G = I_B = 0$

\[
\begin{align*}
V_{GS4} < V_{GS3} < V_{GS2} < V_{GS1} < 0 \\
V_{DS} \\
V_{GS1} \\
V_{GS2} \\
V_{GS3} \\
V_{GS4}
\end{align*}
\]
P-Channel MOSFET: Operation & Model

- You can use the same NMOS model but with absolute values of the all the terminal voltages, currents, and threshold voltage.
- All conditions for operation regions will be the same as NMOS.

\[ |I_D| = \begin{cases} 
0 & |V_{GS}| \leq |V_{TP}| \\
\mu C_{OX} \frac{W}{L} \left( |V_{GS}|-|V_{TP}| - \frac{|V_{DS}|}{2} \right) |V_{DS}| & |V_{GS}| \geq |V_{TP}|, |V_{DS}| < |V_{GS}| - |V_{TP}| \\
\mu C_{OX} \frac{W}{2L} \left( |V_{GS}|-|V_{TP}| \right)^2 \times (1 + \lambda |V_{DS}|) & |V_{GS}| \geq |V_{TP}|, |V_{DS}| \geq |V_{GS}| - |V_{TP}| \\
|V_{TP}| = |V_{TP0}| + \gamma \left( \sqrt{\varphi - |V_{BS}|} - \sqrt{\varphi} \right) &
\end{cases} \]

\[ I_G = I_B = 0 \]
P-Channel MOSFET: Operation & Model

◆ You can use the same NMOS model but with flipping the indices of the terminal voltage notations and the absolute value of the threshold voltage

◆ All conditions for operation regions will be the same as NMOS

\[ I_D = \begin{cases} 
0 & \text{if } V_{SG} \leq |V_{TP}| \\
\mu_P C_{OX} \frac{W}{L} \left( V_{SG} - |V_{TP}| - \frac{V_{SD}}{2} \right) V_{SD} & \text{if } V_{SG} \geq |V_{TP}|, \ V_{SD} < V_{SG} - |V_{TP}| \\
\mu_P C_{OX} \frac{W}{2L} \left( V_{SG} - |V_{TP}| \right)^2 \times (1 + \lambda V_{SD}) & \text{if } V_{SG} \geq |V_{TP}|, \ V_{SD} \geq V_{SG} - |V_{TP}| \\
|V_{TP}| = V_{TP0} + \gamma \left( \sqrt{\phi - V_{SB}} - \sqrt{\phi} \right) & \text{else}
\end{cases} \]

\[ I_G = I_B = 0 \]
MOSFET Modelling: Application Example

- Determine $R_{SW}$ and $C_{GS}$ in the improved switch-level model of an n-channel MOSFET with $L=1\mu m$, $W=1\mu m$ in 0.5$\mu m$ CMOS process using the ideal square-law model.
- Assume $\mu C_{OX}=100\mu A V^{-2}$, $C_{OX}=2.5fF u^{-2}$, $V_{T0}=1V$, $V_{DD}=3.5V$, $V_{SS}=0$, $V_{BS}=0$.

![Diagram of MOSFET with $R_{SW}$ and $C_{GS}$](image-url)

Improved Switch-level model including gate capacitance and drain resistance.
MOSFET Modelling: Application Example

Since the ideal switch-level model is used for digital applications, we will assume deep triode region for computing $R_{SW}$

$$V_{BS} = 0 \rightarrow V_T = V_{T_0}$$

$$I_D = \mu C_{OX} \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS}$$

Deep triode $\rightarrow I_D \approx \mu C_{OX} \frac{W}{L} (V_{GS} - V_T) V_{DS} \rightarrow R_{CH} = \frac{L}{W} \frac{1}{\mu C_{OX} (V_{GS} - V_T)}$

$$R_{SW} = R_{CH} \bigg|_{V_{GS}=3.5V} = \frac{L}{W} \frac{1}{\mu C_{OX} (V_{GS} - V_T)} \bigg|_{V_{GS}=3.5V}$$

$$= \frac{1\mu}{1\mu} \times \frac{1}{100 \times 10^{-6} \text{AV}^{-2} \times (3.5V - 1V)} = 4k\Omega$$

$$C_{GS} = C_{OX} \times L \times W = 2.5fF \text{um}^{-2} \times 1\text{um} \times 1\text{um} = 2.5fF$$
MOSFET Modelling: Application Example

- Determine $R_{SW}$ and $C_{GS}$ in the improved switch-level model of an p-channel MOSFET with $L=1\,\mu\text{m}$, $W=1\,\mu\text{m}$ in 0.5$\mu\text{m}$ CMOS process using the ideal square-law model

- Assume $\mu_p C_{OX}=33\mu \text{AV}^{-2}$, $C_{OX}=2.5f\text{Fu}^{-2}$, $V_{TP0}=-1\text{V}$, $V_{DD}=3.5\text{V}$, $V_{SS}=0$, $V_{SB}=0$

Improved Switch-level model including gate capacitance and drain resistance
MOSFET Modelling: Application Example

Since the ideal switch-level model is used for digital applications, we will assume deep triode region for computing $R_{SW}$

$V_{SB} = 0 \rightarrow V_{Tp} = V_{Tpo}$

$|I_D| = \mu_p C_{OX} \frac{W}{L} \left( V_{SG} - |V_{TP}| - \frac{V_{SD}}{2} \right) V_{SD}$

Deep triode $\rightarrow |I_D| \approx \mu_p C_{OX} \frac{W}{L} \left( V_{SG} - |V_{TP}| \right) V_{SD} \rightarrow R_{CH} = L \frac{1}{W \mu_p C_{OX} \left( V_{SG} - |V_{TP}| \right)}$

$R_{SW} = R_{CH} \Big|_{V_{SG} = 3.5 \text{V}} = L \frac{1}{W \mu_p C_{OX} \left( V_{SG} - |V_{TP}| \right)} \Big|_{V_{SG} = 3.5 \text{V}}$

$= \frac{1 \mu}{1 \mu} \times \frac{1}{33 \times 10^{-6} \text{A} \text{V}^{-2} \times (3.5 \text{V} - 1 \text{V})} = 12k\Omega$

$C_{GS} = C_{OX} \times L \times W = 2.5fF \mu m^{-2} \times 1\mu m \times 1\mu m = 2.5fF$
Basic Devices

- Resistor
- Diode
- Capacitor
- MOSFET
- BJT
Current Carriers in Doped Semiconductors

- Depending on the type of doping in a semiconductor material the current carriers can be dominantly either holes or electrons.
- In a single piece of a semiconductor material, current is conducted through the majority carriers → minority carriers are only short-term carriers.
  - In n-type material → Majority carries are electrons → Minority carriers are holes.
  - In p-type material → Majority carries are holes → Minority carriers are electrons.
  - Either way current is flowing due to the electric field across the material → Drift Current.
How about a complex semiconductor device with multiple types of material?

In a MOSFET Transistor → Current is conducted through the **majority** carriers because of the electric field across the channel → **Drift Current**
How about a complex semiconductor device with multiple types of material?

In a MOSFET Transistor → Current is conducted through the **majority** carriers because of the electric field across the channel → **Drift Current**

![Diagram of a MOSFET with current flow through the channel](image-url)
Current Carriers in Complex Devices

- How about a complex semiconductor device with multiple types of material?
- In a Diode → Current is conducted through the minority carriers around the junction because of the difference in carrier concentration → Diffusion Current

Holes invade the n-type material and cause current flow in the n-type side → Current flow in the n-type side is through minority carriers immediately after the junction. Deep in the material majority carriers take over.

Electrons invade the p-type material and cause current flow in the p-type side → Current flow in the p-type side is through minority carriers immediately after the junction. Deep in the material majority carriers take over.
Bipolar Transistors: Basic Operation

- Bipolar devices are stacks of 3 layers of different types of semiconductor materials \(\rightarrow\) Darker colors mean heavier doping levels
- They show basic symmetry, but their electric properties are not \(\rightarrow\) Which is the Collector and which is the Emitter is actually critical \(\rightarrow\) Compare to MOSFETs
Bipolar Transistors: Basic Operation

- As opposed to MOSFETs, BJT are 3-terminal devices and not 4-terminal devices

![pnp transistor](image1)

![npn transistor](image2)

n-channel MOSFET

p-channel MOSFET
NPN Bipolar Transistors: Basic Operation

- At a first glance it may appear that it is impossible for any current to flow between the Collector and Emitter because of the back-to-back diode structure → this is true EXCEPT if the base thickness is very small
NPN Bipolar Transistors: Basic Operation

- Let’s apply a positive voltage across the Base Emitter Junction and also the Collector Emitter Junction and see what happens if the base is very thick.
- When electrons diffuse into the base from the emitter, they get attacked by the large number of holes in the base. If the gate is very thick, electrons will completely be recombined with holes before they ever make it to the collector. In this case, the current flow in the emitter will be sustained by only the base and there will be no current flow between the collector and the emitter.

\[ I_B = -I_E \]
\[ I_C = 0 \]
Let’s apply a positive voltage across the Base Emitter Junction and also the Collector Emitter Junction and see what happens if the base is very thin.

When electrons diffuse into the base from the emitter, they get attacked by the large number of holes in the base → if the gate is very thin, some electrons will be recombined with holes, but most of them will make it to the collector → In this case, the current flow in the emitter will be sustained partially by the base terminal and mostly by the collector terminal (despite the fact that the collector-base junction is reverse biased).

\[ I_C + I_B = -I_E \]
\[ I_C \neq 0 \]

\[ I_E \]
NPN Bipolar Transistors: Basic Operation

- The portion of the charge diffusing from the emitter into the base and making it to the collector is termed \( \alpha \rightarrow \) It is always less than 1, but for good transistors it is \( 0.99 < \alpha < 0.999 \rightarrow \) making the base thinner makes \( \alpha \) bigger
- The flow of current from the collector to the emitter is sustained by minority carriers in the base region

\[
I_C + I_B = -I_E \\
I_C = -\alpha I_E
\]
NPN Bipolar Transistors: Basic Operation

\[ I_C + I_B = -I_E \]

\[ I_C = -\alpha I_E \]

\[ I_B = -(1 - \alpha) I_E \]

\[ I_C = \frac{\alpha}{1 - \alpha} I_B \]

\[ \beta = \frac{\alpha}{1 - \alpha} \]

\[ I_C = \beta I_B \]

\( \beta \) is typically very large

often \( 50 < \beta < 999 \)
NPN Bipolar Transistors: Basic Operation

- The Bipolar Transistor can be thought of a current amplifier with a large current gain \( \rightarrow \) In contrast to a MOS transistor, which is inherently a transconductance amplifier.

- Current flow in base is governed by the diode equation \( \rightarrow \) \( I_B = I_S e^{\frac{V_{BE}}{V_t}} \)

- This means that the Collector current varies exponentially with \( V_{BE} \)

\[
I_C = \beta \tilde{I}_S e^{\frac{V_{BE}}{V_t}}
\]
The exponential relationship (in contrast to the square-law relationship for the MOSFET) between $V_{BE}$ and the Collector current provides a very large gain for the BJT and this property is very useful for many applications!!

High gain means that for a small variation in $V_{BE}$, the change in $I_C$ is going to be large.

Exponential relationships have much higher gain than square-law.
We will consider $I_B$ and $I_C$ dependent variables, while $V_{BE}$ and $V_{CE}$ as the independent variables.

We will also consider that all the terminal currents are positive when they are flowing into the terminals.
NPN Bipolar Transistors: Modelling

Note that as in the diode case, the saturation current from the emitter-base junction is a function of the junction area (the emitter area in BJTs) \[ I_{SE} = J_S A_E \]

This saturation current will be divided between the base and collector terminals using by the same \( \alpha \) factor between \( I_C \) and \( I_B \)

\[ \tilde{I}_S = (1 - \alpha) J_S A_E = \left( \beta + 1 \right)^{-1} J_S A_E \approx \beta^{-1} J_S A_E \]
NPN Bipolar Transistors: Modelling

\[ I_B = I_S e^{\frac{V_{BE}}{V_t}} \]

\[ I_C = \beta I_S e^{\frac{V_{BE}}{V_t}} \]

\[ V_t = \frac{kT}{q} \]

\[ I_B = \frac{J_S A_E}{\beta} e^{\frac{V_{BE}}{V_t}} \]

\[ I_C = J_S A_E e^{\frac{V_{BE}}{V_t}} \]

\[ V_t = \frac{kT}{q} \]

- \(J_S\) is termed the saturation current density
- Process parameters \(\rightarrow J_S, \beta\)
- Design parameters \(\rightarrow A_E\)
- Environmental parameters and physical constants \(\rightarrow k, T, q\)
- At room temp. \(\rightarrow V_t\) is about 26mV
- \(J_S\) is very small \(\rightarrow\) around 0.25fA/\(\mu\)m\(^2\)
NPN Bipolar Transistors: Modelling

- Same as with diodes → $V_{BE}$ close to 0.6V for a two decade change in $I_C$

$$J_S = 0.25 fA/u^2$$
$$A_E = 400 u^2$$
NPN Bipolar Transistors: Modelling

- Even for four decade change in $I_C$, $V_{BE}$ is still close to 0.6V

$J_S = 0.25 \text{fA/}u^2$

$A_E = 400u^2$

![Graph showing the relationship between $I_C$ (mA) and $V_{BE}$](image-url)
According to our model, $I_C$ is actually not a function of $V_{CE}$ → It is only a function of either $V_{BE}$ or $I_B$ → this region of operation is referred to as the Forward Active Region

It is similar to the Saturation Region of the MOSFET

$$I_B = \frac{J_S A_E}{\beta} e^{\frac{V_{BE}}{V_t}}$$

$$I_C = J_S A_E e^{\frac{V_{BE}}{V_t}} = \beta I_B$$

$V_t = \frac{kT}{q}$

Valid only in Forward Active Region
NPN Bipolar Transistors: Saturation

- In Forward Active region, $I_C$ is not a function of $V_{CE}$ → It is only a function of either $V_{BE}$ or $I_B$
- But this is only true at high $V_{CE}$ → at lower values of $V_{CE}$, the base collector junction starts to turn on, which causes the collector current to drop→ This is referred to as the Saturation Region of operation
- It is similar to the Triode region of the MOSFET

![Diagram of NPN Bipolar Transistor](image-url)

- $V_{CE}$
- $I_C$
- $V_{BE}$ or $I_B$
NPN Bipolar Transistors: Saturation

- The Saturation region in BJT is similar to the Triode region of the MOSFET → But we do not have a mathematical model for it yet
If $V_{BE}$ becomes much less than 0.6V, the transistor operates in the cutoff region regardless of $V_{CE}$.
NPN Bipolar Transistors: Nonidealities

- There are some nonidealities that must be accounted for in the Forward Active region.
- The collector current changes a little bit with $V_{CE} \rightarrow$ Projections of the tangential lines all intercept the $-V_{CE}$ axis at the same place and this is termed the Early voltage ($V_{AF}$).
- $V_{AF}$ is in the 100V range $\rightarrow$ is that better or worse than MOSFET?

\[
I_B = \frac{J_S A_E}{\beta} e^{\frac{V_{BE}}{V_t}}
\]

\[
I_C = J_S A_E e^{\frac{V_{BE}}{V_t}} \left( 1 + \frac{V_{CE}}{V_{AF}} \right)
\]

\[
V_t = \frac{kT}{q}
\]

Valid only in Forward Active Region
NPN Bipolar Transistors: Comprehensive Model

- We need a model that describes the entire operation of BJT \( \rightarrow \) Ebers-Moll Model
- Valid in all regions \( \rightarrow \) The \( V_{AF} \) effect can be added exactly as before
- \( \alpha_F \) is the portion of the emitter current that goes to the collector
- \( \alpha_R \) is the portion of the collector current that goes to the emitter if the transistor is flipped over

\[
I_E = -\frac{J_S A_E}{\alpha_F} \left( e^{\frac{V_{BE}}{V_t}} - 1 \right) + J_S A_E \left( e^{\frac{V_{BC}}{V_t}} - 1 \right)
\]

\[
I_C = J_S A_E \left( e^{\frac{V_{BE}}{V_t}} - 1 \right) - \frac{J_S A_E}{\alpha_R} \left( e^{\frac{V_{BC}}{V_t}} - 1 \right)
\]

\[
I_C + I_B = -I_E
\]

\[
V_t = \frac{kT}{q}
\]

Valid in all Regions
**NPN Bipolar Transistors: Comprehensive Model**

- The Ebers-Moll Model describes $I_C$ and $I_E$ in terms of $V_{BE}$ and $V_{BC}$, $\alpha_F$, and $\alpha_R \rightarrow$ but we can also express it in terms of $V_{BE}$, $V_{CE}$, $\beta_F$, $\beta_R$ to be consistent with our previous notation.

- Take into account that the exponent of $V_{BE}$ and is much larger than one.

\[
I_E = -\frac{J_S A_E}{\alpha_F} \left( e^{\frac{V_{BE}}{V_t}} - 1 \right) + J_S A_E \left( e^{\frac{V_{BC}}{V_t}} - 1 \right) \approx -J_S A_E e^{\frac{V_{BE}}{V_t}} \left( \frac{1}{\alpha_F} - \frac{-V_{CE}}{V_t} - e^{\frac{-V_{BE}}{V_t}} \right)
\]

\[
I_C = J_S A_E \left( e^{\frac{V_{BE}}{V_t}} - 1 \right) - \frac{J_S A_E}{\alpha_R} \left( e^{\frac{V_{BC}}{V_t}} - 1 \right) \approx J_S A_E e^{\frac{V_{BE}}{V_t}} \left( 1 - \frac{1}{\alpha_R} \right) \left( e^{\frac{-V_{CE}}{V_t}} - e^{\frac{-V_{BE}}{V_t}} \right)
\]

\[
I_C + I_B = -I_E
\]

\[
\beta_F \overset{defn}{=} \frac{\alpha_F}{1 - \alpha_F}, \quad \beta_R \overset{defn}{=} \frac{\alpha_R}{1 - \alpha_R}
\]
The Ebers-Moll Model describes $I_C$ and $I_E$ in terms of $V_{BE}$ and $V_{BC}$, $\alpha_F$, and $\alpha_R$ but we can also express it in terms of $V_{BE}$, $V_{CE}$, $\beta_F$, $\beta_R$ to be consistent with our previous notation.

$$I_B = \frac{J_S A_E}{\beta_F} \frac{V_{BE}}{V_t} \left( 1 + \frac{\beta_F}{\beta_R} e^{-\frac{V_{CE}}{V_t}} \right)$$

$$I_C = J_S A_E \frac{V_{BE}}{V_t} \left( 1 - \left[ \frac{1 + \beta_R}{\beta_R} \right] e^{-\frac{V_{CE}}{V_t}} \right)$$

$$V_t = \frac{kT}{q}$$
NPN Bipolar Transistors: Comprehensive Model

- In Forward Active $\rightarrow V_{CE} > V_{BE}$ (0.4V-0.7V) $\rightarrow$ the exponent with $V_{CE}$ is so small

\[ I_B = \frac{J_S A_E}{\beta_F} e^{\frac{V_{BE}}{V_t}} \left( 1 + \frac{\beta_F}{\beta_R} e^{-\frac{V_{CE}}{V_t}} \right) \]

\[ I_C = J_S A_E e^{\frac{V_{BE}}{V_t}} \left( 1 - \left[ 1 + \frac{\beta_R}{\beta_F} \right] e^{-\frac{V_{CE}}{V_t}} \right) \]

\[ V_t = \frac{kT}{q} \]

\[ I_B = \frac{J_S A_E}{\beta_F} e^{\frac{V_{BE}}{V_t}} \]

\[ I_C = J_S A_E e^{\frac{V_{BE}}{V_t}} \]

\[ V_t = \frac{kT}{q} \]

Same Forward Active model we developed before
In Saturation → $V_{CE} < V_{BE}(0.4V-0.7V)$ → the exponent with $V_{CE}$ approaches “1” very quickly and $I_C$ drops very rapidly

$$I_B = \frac{J_S A_E}{\beta_F} e^{\frac{V_{BE}}{V_t}} \left(1 + \frac{\beta_F}{\beta_R} e^{-\frac{V_{CE}}{V_t}}\right)$$

$$I_C = J_S A_E e^{\frac{V_{BE}}{V_t}} \left(1 - \left[1 + \frac{\beta_R}{\beta_F}\right] e^{-\frac{V_{CE}}{V_t}}\right)$$

When $V_{CE} = 0$

$$I_B = J_S A_E e^{\frac{V_{BE}}{V_t}} \left(\frac{1}{\beta_F} + \frac{1}{\beta_R}\right)$$

$$I_C = J_S A_E e^{\frac{V_{BE}}{V_t}} \left(-\frac{1}{\beta_R}\right)$$

$$V_t = \frac{kT}{q}$$
NPN Bipolar Transistors: Ebers-Moll Model

- The Ebers-Moll Model with the $V_{AF}$ effect

\[ I_B = \frac{J_S A_E}{\beta_F} e^{\frac{V_{BE}}{V_t}} \left( 1 + \frac{\beta_F}{\beta_R} e^{-\frac{V_{CE}}{V_t}} \right) \]

\[ I_C = J_S A_E e^{\frac{V_{BE}}{V_t}} \left( 1 - \left[ \frac{1 + \beta_R}{\beta_R} \right] e^{-\frac{V_{CE}}{V_t}} \right) \left( 1 + \frac{V_{CE}}{V_{AF}} \right) \]

\[ V_t = \frac{kT}{q} \]
Observe that $V_{CE}$ is around 0.2V when in the saturation region

$V_{BE}$ is around 0.6V when in the saturation region

In most applications, exact $V_{CE}$ and $V_{BE}$ voltages in saturation are not critical

Therefore, in saturation region we simply assume:

$V_{BE} = 0.7V$

$V_{CE} = 0.2V$

Saturation
NPN Bipolar Transistors: Simplified Multi-Region Model

Ebers-Moll Model

\[ I_B = \frac{J_S A_E}{\beta_F} e^{\frac{V_{BE}}{V_t}} \left( 1 + \frac{\beta_F}{\beta_R} e^{\frac{-V_{CE}}{V_t}} \right) \]

\[ I_C = J_S A_E e^{\frac{V_{BE}}{V_t}} \left( 1 - \left[ 1 + \frac{\beta_R}{\beta_F} e^{\frac{-V_{CE}}{V_t}} \right] \right) \left( 1 + \frac{V_{CE}}{V_{AF}} \right) \]

\[ V_t = \frac{kT}{q} \]

Simplified Multi-Region Model

\[ I_B = \frac{J_S A_E}{\beta_F} e^{\frac{V_{BE}}{V_t}} \]

\[ I_C = J_S A_E e^{\frac{V_{BE}}{V_t}} \left( 1 + \frac{V_{CE}}{V_{AF}} \right) = \beta_F I_B \left( 1 + \frac{V_{CE}}{V_{AF}} \right) \rightarrow \text{Forward Active} \]

\[ V_{BE} = 0.7V, \quad V_{CE} = 0.2V \rightarrow \text{Saturation} \]

\[ I_B = 0, \quad I_C = 0 \rightarrow \text{Cuttoff} \]
NPN Bipolar Transistors: Simplified Multi-Region Model

\[ I_C = J_S A E \frac{V_{BE}}{V_t} \left( 1 + \frac{V_{CE}}{V_{AF}} \right) \]

\[ I_B = J_S A E \frac{V_{BE}}{V_t} \frac{\beta}{\beta} \]

\[ V_t = \frac{kT}{q} \]

\[ V_{BE} > 0.4V \]

\[ V_{BC} < 0 \rightarrow V_{CE} > V_{BE} \]

Forward Active

\[ V_{BE} = 0.7V \]

\[ V_{CE} = 0.2V \]

Saturation

\[ I_C < \beta I_B \]

\[ I_C = I_B = 0 \]

Cutoff

\[ V_{BE} < 0 \]

\[ V_{BC} < 0 \rightarrow V_{CE} > V_{BE} \]

A small portion of the operating region is missed with this model but seldom operate in the missing region.
NPN Bipolar Transistors: Simplified Multi-Region Model

\[ I_C = \beta I_B \left( 1 + \frac{V_{CE}}{V_{AF}} \right) \]

\[ I_B = \frac{J_S A_E}{\beta} \frac{V_{BE}}{V_t} \]

\[ V_t = \frac{kT}{q} \]

- \[ V_{BE} > 0.4V \]
  - Forward Active
  - \[ V_{BC} < 0 \rightarrow V_{CE} > V_{BE} \]

- \[ V_{BE} = 0.7V \]
  - Saturation
  - \[ I_C < \beta I_B \]
  - \[ V_{CE} = 0.2V \]

- \[ I_C = I_B = 0 \]
  - Cutoff
  - \[ V_{BC} < 0 \rightarrow V_{CE} > V_{BE} \]

An alternative representation of the simplified multi-region model
In Forward Active, the device behaves like a **nonideal CCCS** between the collector and the emitter.

\[
I_C = \beta I_B \left( 1 + \frac{V_{CE}}{V_{AF}} \right) = \beta I_B + \beta I_B \frac{V_{CE}}{V_{AF}} = I_{CEQ} + \frac{V_{CE}}{R_{CEQ}}
\]

\[
R_{CEQ} = \frac{V_{AF}}{I_{CEQ}} \approx \frac{V_{AF}}{I_C}
\]

Adequate when it makes little difference whether \( V_{BE} = 0.6V \) or \( V_{BE} = 0.7V \).
NPN Bipolar Transistors: Simplified Multi-Region Model

- Various operation regions in the multi-region model

Seldom operate in regions excluded in this picture
What happens if the base-emitter or base-collector junctions experience large forward bias?
Bipolar Versus MOSFET Transistors: A Comparison

- **The general characteristics are very similar**

- **Forward Active region of a BJT is similar to Saturation region in a MOSFET** → A BJT acts as a current amplifier, while a MOSFET acts as a transconductance amplifier

- **Saturation region of a BJT is similar to Triode region in a MOSFET** → the slope versus $V_{CE}$ is much steeper than the slope versus $V_{DS}$

- **Spacing between regions is different (Exponential vs square law)**
Other MOS and Bipolar Devices

- Depletion MOSFETs
- JFETs
- Schottky Diodes
- MESFETs
- Thyristors: SCR, TRIAC
Depletion versus Enhancement MOSFETs

- The MOSFET transistors we studied so far are referred to as Enhancement Mode devices
  - For NMOS $\Rightarrow V_T > 0$
  - For PMOS $\Rightarrow V_T < 0$
- In an Enhancement Mode MOSFET a voltage must be applied on the gate to create the channel $\Rightarrow$ They are naturally “off” devices
- Depletion Mode MOSFETs have a physical channel already existing $\Rightarrow$ They are naturally “on” devices
  - For NMOS $\Rightarrow V_T < 0$
  - For PMOS $\Rightarrow V_T > 0$
Depletion versus Enhancement MOSFETs

- Depletion mode devices require one additional mask.
- Older NMOS and PMOS processes usually had depletion device and enhancement device of the same type to compensate for not having a complementary device.
- Depletion devices usually not available in CMOS because applications usually do not justify the small increasing costs in processing.

[Diagrams of Enhancement and Depletion MOSFETs]
The JFET

- The JFET is a device that controls its channel through depletion region control rather than channel inversion.
- Depletion region control can be done through reverse bias voltage.

Triode Region → Channel becomes thinner as the gate voltage increases.
The JFET

- The JFET is a device that controls its channel through depletion region control rather than channel inversion.
- Deletion region control can be done through reverse bias voltage.

Saturation Region → Channel pinches off as the drain voltage increases.
The JFET

Functionally identical to the square-law model of MOSFET

Parameters $I_{DSS}$ and $V_P$ characterize the device

$I_{DSS}$ proportional to $W/L$ where $W$ and $L$ are width and length of n+ diff

Square-law model of n-channel JFET

$$I_D = \begin{cases} 
0 & V_{GS} < V_P \\
\frac{2I_{DSS}^2}{V_P^2} \left( V_{GS} - V_P - \frac{V_{DS}}{2} \right) V_{DS} & V_{GS} > V_P, \quad V_{DS} < V_{GS} - V_P \\
I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2 & V_{GS} > V_P, \quad V_{DS} < V_{GS} - V_P
\end{cases}$$
The JFET

Square-law model of n-channel JFET

\[
I_D = \begin{cases} 
0 & \text{if } V_{GS} < V_P \\
\frac{2I_{DSS}V_P^2}{V_P^2} \left(V_{GS} - V_P - \frac{V_{DS}}{2}\right) V_{DS} & \text{if } V_{GS} > V_P, \quad V_{DS} < V_{GS} - V_P \\
I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2 & \text{if } V_{GS} > V_P, \quad V_{DS} < V_{GS} - V_P
\end{cases}
\]

- \( V_P \) is negative for n-channel device, positive for p-channel device \( \rightarrow \) JFET is a depletion mode device
- Must not forward bias GS junction by over 300mV or excessive base current will flow
- Widely used as input stage for bipolar op-amps
The Schottky Diode

- Metal-Semiconductor Junction
- One contact is Ohmic, other is rectifying
- Not available in all processes
- Relatively inexpensive adder in some processes
- Lower threshold voltage than pn junction diode $\Rightarrow 0.15V–0.45V$
- High speed
The MESFET

- Metal-Semiconductor Junction for Gate
- Drain and Source contacts ohmic, other is rectifying
- Usually not available in standard CMOS processes
- Must not forward bias very much
- Lower threshold voltage than pn junction diode
- High speed