EE330
Integrated Electronics

Spring 2014

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Director, Power Management Research Lab
Electrical & Computer Engineering, Iowa State University
Course Information

◆ Lecture Instructor
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Director, Power Management Research Lab
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Web: http://home.eng.iastate.edu/~aafayed/
Class Website: http://home.eng.iastate.edu/~aafayed/ee330
Office hours: Mondays and Wednesdays 10:30am to 11:30am at 2117 Coover Hall

◆ Lab Instructors
Wenbing Ma <mwb1992@iastate.edu>, Sections A, D
Craig Gustafson <craigg@iastate.edu>, Sections C, E
Yunxi Guo <yunxig@iastate.edu>, Sections F, HW Grading
Course Information

◆ Lectures
Mondays, Wednesdays, and Fridays from 9:00am to 9:50am
0268 Carver Hall

◆ Lab Sections
Section A: Tuesday 8:00am to 10:50am, Coover 2046
Section B: Cancelled
Section C: Thursday 3:10pm to 6:00pm, Coover 2046
Section D: Wednesday 3:10pm to 6:00pm, Coover 2046
Section E: Friday 1:10pm to 4:00pm, Coover 2046
Section F: Friday 10:00am to 12:50pm, Coover 2046
Section G: Cancelled
Course Information: Catalog Description

E E 330. Integrated Electronics. (Same as Cpr E 330.) (3-3)
Cr. 4. F.S. Prereq: 201, credit or enrollment in 230, Cpr E 210

Course Information: Topics Covered

◆ Semiconductor Processes
◆ Device Models (Diode, MOSFET, BJT, Thyristor)
◆ Device Layout
◆ Simulation and Verification
◆ Basic Digital Building Blocks
◆ Behavioral Design and Synthesis
  ▶ Standard cells
◆ Basic Analog Building Blocks
Course Information: Textbook

- CMOS VLSI Design – A Circuits and Systems Perspective by Weste and Harris Addison Wesley/Pearson, 2011 → Fourth Edition
Course Information: Other Textbooks
This class has a substantial hands-on laboratory section. Students will be using expensive, sensitive, and potentially hazardous test equipment. Safety in the lab is a number one priority for students and instructors and to ensure a safe laboratory experience, a brief safety presentation will be given the first day of lab and students will have to sign a safety orientation form posted on the class website and submit it to the lab instructor before starting the first lab. It is mandatory that all students attend the presentation and sign the form. Moreover, it is expected that students follow any and all posted safety guidelines. For reference, a copy of the University Laboratory Safety Manual can be found at:

Course Information: Grading Policy

- **Homework → 100 points (1/6 of total course points)**
  - One homework assignment every week (14 assignments in total)

- **Lab & Lab Reports → 100 points (1/6 of total course points)**

- **Project → 100 points (1/6 of total course points)**

- **3 Midterms → 100 points (1/6 of total course points)**

- **1 Final → 100 points (1/6 of total course points)**

- **Attendance/Quizzes → 100 points (1/6 of total course points)**

- Please check class website for more details on grading policies
Course Information: Grading Policy

◆ Lab Attendance Policy → Without a legitimate excuse
  ➢ Each missed session deducts 50 points of the total course points
  ➢ Missing two sessions will earn you zero points for the lab portion
  ➢ Missing further sessions will earn you negative credit and will very easily earn you an “F” grade regardless of your performance in the other portions of the course

◆ Lecture Attendance Policy → Without a legitimate excuse
  ➢ Will call 5 or more names randomly each lecture
  ➢ Missing a lecture deducts 25 points of the total course points
  ➢ Missing 4 lectures will earn you zero points for the attendance portion
  ➢ Missing further lectures will NOT impose a negative credit
  ➢ If you are missing once, your name will be very likely called in future lectures
The Semiconductor Industry
The Semiconductor Industry

◆ What is it?
◆ How big is it?

<table>
<thead>
<tr>
<th>Year</th>
<th>Sales</th>
</tr>
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<tbody>
<tr>
<td>1984</td>
<td>$25B</td>
</tr>
<tr>
<td>1990</td>
<td>$50B</td>
</tr>
<tr>
<td>1994</td>
<td>$100B</td>
</tr>
<tr>
<td>2004</td>
<td>$200B</td>
</tr>
<tr>
<td>2010</td>
<td>$304B</td>
</tr>
<tr>
<td>2012</td>
<td>$336B (projected)</td>
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</table>

Semiconductor sales do not include the sales of the electronic systems in which they are installed and this market is much bigger!!
The Semiconductor Industry

Gartner Revised Semiconductor Growth Forecast June-08

The Semiconductor Industry

◆ How does it compare to other industries?
◆ Iowa-centric industries (lots and lots of food!)
  ➢ First in Corn, Soybean, Egg, and Hog production, Second in Red Meat

### Corn Production

<table>
<thead>
<tr>
<th></th>
<th>Bushels (Billions)</th>
<th>Value (Billion Dollars)</th>
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</thead>
<tbody>
<tr>
<td>Iowa</td>
<td>2.24</td>
<td>$3.98</td>
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<tr>
<td>United States</td>
<td>11.8</td>
<td>$21.0</td>
</tr>
<tr>
<td>World</td>
<td>23.3</td>
<td>$41.5</td>
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</table>

### Soybean Production

<table>
<thead>
<tr>
<th></th>
<th>Bushels (Millions)</th>
<th>Value (Billion Dollars)</th>
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</thead>
<tbody>
<tr>
<td>Iowa</td>
<td>338</td>
<td>$1.65</td>
</tr>
<tr>
<td>United States</td>
<td>3,141</td>
<td>$15.4</td>
</tr>
<tr>
<td>World</td>
<td>7,968</td>
<td>$39.0</td>
</tr>
</tbody>
</table>

http://www.iowalifec.../travel/iowafacts/statistics.html

World 2006 semiconductor sales of $235B approx. 300% larger than total corn and soybean production for many years!
The Semiconductor Industry

◆ What is it → All electronic circuits

◆ How big is it → About $335B/Year and growing in spite of economic downturn

◆ How does it compare to Iowa-centric industries → Larger than major agricultural commodities (1.4X to 3X)

◆ The semiconductor industry is one of the largest sectors in the world economy and continues to grow
The Semiconductor Industry: The Big Players

Source: IHS iSuppli Semiconductor preliminary rankings for 2011

(foundries excluded)

<table>
<thead>
<tr>
<th>Rank 2011</th>
<th>Rank 2010</th>
<th>Company</th>
<th>Country of origin</th>
<th>Revenue (million $ USD)</th>
<th>2011/2010 changes</th>
<th>Market share</th>
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<tr>
<td>1</td>
<td>1</td>
<td>Intel Corporation(1)</td>
<td>USA</td>
<td>49,685</td>
<td>+23.0%</td>
<td>15.9%</td>
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<tr>
<td>2</td>
<td>2</td>
<td>Samsung Electronics</td>
<td>South Korea</td>
<td>29,242</td>
<td>+3.0%</td>
<td>9.3%</td>
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<tr>
<td>3</td>
<td>4</td>
<td>Texas Instruments(2)</td>
<td>USA</td>
<td>14,081</td>
<td>+8.4%</td>
<td>4.5%</td>
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<td>4</td>
<td>3</td>
<td>Toshiba Semiconductor</td>
<td>Japan</td>
<td>13,362</td>
<td>+2.7%</td>
<td>4.3%</td>
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<tr>
<td>5</td>
<td>5</td>
<td>Renesas Electronics</td>
<td>Japan</td>
<td>11,153</td>
<td>-6.2%</td>
<td>3.6%</td>
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<tr>
<td>6</td>
<td>9</td>
<td>Qualcomm(3)</td>
<td>USA</td>
<td>10,080</td>
<td>+39.9%</td>
<td>3.2%</td>
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<tr>
<td>7</td>
<td>7</td>
<td>STMicroelectronics</td>
<td>Italy, France</td>
<td>9,792</td>
<td>-5.4%</td>
<td>3.1%</td>
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<tr>
<td>8</td>
<td>6</td>
<td>Hynix</td>
<td>South Korea</td>
<td>8,911</td>
<td>+69.3%</td>
<td>3.5%</td>
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<tr>
<td>9</td>
<td>8</td>
<td>Micron Technology</td>
<td>USA</td>
<td>7,344</td>
<td>+106.2%</td>
<td>2.9%</td>
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<tr>
<td>10</td>
<td>10</td>
<td>Broadcom</td>
<td>USA</td>
<td>7,153</td>
<td>+52.1%</td>
<td>2.1%</td>
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<tr>
<td>11</td>
<td>12</td>
<td>Advanced Micro Devices</td>
<td>USA</td>
<td>6,483</td>
<td>+22.0%</td>
<td>2.1%</td>
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<tr>
<td>12</td>
<td>13</td>
<td>Infineon Technologies</td>
<td>Germany</td>
<td>5,403</td>
<td>+39.7%</td>
<td>2.0%</td>
</tr>
<tr>
<td>13</td>
<td>14</td>
<td>Sony</td>
<td>Japan</td>
<td>5,153</td>
<td>+19.4%</td>
<td>1.8%</td>
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<tr>
<td>14</td>
<td>16</td>
<td>Freescale Semiconductor</td>
<td>USA</td>
<td>4,485</td>
<td>+27.2%</td>
<td>1.4%</td>
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<tr>
<td>15</td>
<td>11</td>
<td>Elpida Memory</td>
<td>Japan</td>
<td>3,854</td>
<td>+74.2%</td>
<td>1.2%</td>
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<tr>
<td>16</td>
<td>17</td>
<td>NXP</td>
<td>Netherlands</td>
<td>3,836</td>
<td>+24.1%</td>
<td>1.2%</td>
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<tr>
<td>17</td>
<td>20</td>
<td>NVIDIA</td>
<td>USA</td>
<td>3,672</td>
<td>+12.8%</td>
<td>1.2%</td>
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<tr>
<td>18</td>
<td>18</td>
<td>Marvell Technology Group</td>
<td>USA</td>
<td>3,448</td>
<td>+43.1%</td>
<td>1.1%</td>
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<tr>
<td>19</td>
<td>26</td>
<td>ON Semiconductor(4)</td>
<td>USA</td>
<td>3,423</td>
<td>+49.4%</td>
<td>1.1%</td>
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<tr>
<td>20</td>
<td>15</td>
<td>Panasonic Corporation</td>
<td>Japan</td>
<td>3,365</td>
<td>+58.1%</td>
<td>1.1%</td>
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</tbody>
</table>
The Semiconductor Industry: Applications

- Communication systems
- Computation systems
- Instrumentation and control
- Signal processing
- Biomedical devices
- Automotive
- Entertainment
- Military
- Many-many more

Electronic circuit designers must understand system operation to provide useful electronic solutions.
Electronic Circuits: The Basic Building Block

The Transistor!

- A fundamental component for building electronic circuits
- Described in terms of feature size → the minimum lateral dimensions of the transistor that can be fabricated in a given semiconductor process → aka minimum transistor gate length
- The smaller the feature size, the more circuits we can build within a given area

Bounding region often a factor of 10 or more larger than area of transistor itself
The Transistor: Moore’s Law

◆ From Wikipedia

➢ Moore's law is the empirical observation that the complexity of integrated circuits, with respect to minimum component cost, doubles every 24 months. It is attributed to Gordon E. Moore, a co-founder of Intel

➢ Often misinterpreted or generalized

➢ Many say it has been dead for several years

➢ Many say it will continue for a long while

➢ Not intended to be a long-term prophecy

◆ Regardless, device scaling, device count, and circuit complexity will continue to dramatically improve for the foreseeable future even if they don’t follow Moore’s law exactly
The Transistor: Technology Predictions

- International Technology Roadmap for Semiconductors (ITRS) Technology Predictions → feature length

![Graph showing minimum gate length predictions from 2000 to 2020](image)
The Transistor: Technology Predictions

- International Technology Roadmap for Semiconductors (ITRS)
  Technology Predictions $\rightarrow$ supply voltage

ITRS 2004 Supply Voltage Predictions

YEAR:
- 2000
- 2005
- 2010
- 2015
- 2020

Supply Voltage Levels:
- 3.5
- 3
- 2.5
- 2
- 1.5
- 1
- 0.5
- 0
Some Semiconductor Trends

- Microprocessors
- Memory
- Data rate for wireless and wire-line serial communication
# Some Semiconductor Trends: Microprocessors

[Main article: microprocessor chronology](http://en.wikipedia.org/wiki/Transistor_count)

<table>
<thead>
<tr>
<th>Processor</th>
<th>Transistor count</th>
<th>Date of introduction</th>
<th>Manufacturer</th>
<th>Process</th>
<th>Area</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel 4004</td>
<td>2,300</td>
<td>1971</td>
<td>Intel</td>
<td>10 μm</td>
<td>12 mm²</td>
</tr>
<tr>
<td>Intel 8008</td>
<td>3,500</td>
<td>1972</td>
<td>Intel</td>
<td>10 μm</td>
<td>14 mm²</td>
</tr>
<tr>
<td>MOS Technology 6502</td>
<td>3,510</td>
<td>1975</td>
<td>MOS Technology</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Motorola 6800</td>
<td>4,100</td>
<td>1974</td>
<td>Motorola</td>
<td></td>
<td>16 mm²</td>
</tr>
<tr>
<td>Intel 8080</td>
<td>4,500</td>
<td>1974</td>
<td>Intel</td>
<td>6 μm</td>
<td>20 mm²</td>
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<tr>
<td>RCA 1802</td>
<td>5,000</td>
<td>1974</td>
<td>RCA</td>
<td>5 μm</td>
<td>27 mm²</td>
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<tr>
<td>Intel 8085</td>
<td>6,500</td>
<td>1976</td>
<td>Intel</td>
<td>3 μm</td>
<td>20 mm²</td>
</tr>
<tr>
<td>Zilog Z80</td>
<td>8,500</td>
<td>1976</td>
<td>Zilog</td>
<td>4 μm</td>
<td>18 mm²</td>
</tr>
<tr>
<td>Motorola 6809</td>
<td>9,000</td>
<td>1978</td>
<td>Motorola</td>
<td>5 μm</td>
<td>21 mm²</td>
</tr>
<tr>
<td>Intel 8086</td>
<td>29,000</td>
<td>1978</td>
<td>Intel</td>
<td>3 μm</td>
<td>33 mm²</td>
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<tr>
<td>Intel 8088</td>
<td>29,000</td>
<td>1979</td>
<td>Intel</td>
<td>3 μm</td>
<td>33 mm²</td>
</tr>
<tr>
<td>Intel 80186</td>
<td>55,000</td>
<td>1982</td>
<td>Intel</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Motorola 68000</td>
<td>68,000</td>
<td>1979</td>
<td>Motorola</td>
<td>4 μm</td>
<td>44 mm²</td>
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<tr>
<td>Intel 80286</td>
<td>134,000</td>
<td>1982</td>
<td>Intel</td>
<td>1.5 μm</td>
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</tr>
<tr>
<td>Intel 80386</td>
<td>275,000</td>
<td>1985</td>
<td>Intel</td>
<td>1.5 μm</td>
<td>104 mm²</td>
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<tr>
<td>Intel 80486</td>
<td>1,180,000</td>
<td>1989</td>
<td>Intel</td>
<td>1 μm</td>
<td></td>
</tr>
<tr>
<td>Pentium</td>
<td>3,100,000</td>
<td>1993</td>
<td>Intel</td>
<td>0.8 μm</td>
<td></td>
</tr>
<tr>
<td>AMD K5</td>
<td>4,300,000</td>
<td>1996</td>
<td>AMD</td>
<td>0.5 μm</td>
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<tr>
<td>Pentium II</td>
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<td>1997</td>
<td>Intel</td>
<td>0.35 μm</td>
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<tr>
<td>AMD K6</td>
<td>8,800,000</td>
<td>1997</td>
<td>AMD</td>
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<tr>
<td>Pentium III</td>
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<td>1999</td>
<td>Intel</td>
<td>0.25 μm</td>
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</table>
## Some Semiconductor Trends: Microprocessors

<table>
<thead>
<tr>
<th>Processor</th>
<th>Transistor count</th>
<th>Date of introduction</th>
<th>Manufacturer</th>
<th>Process</th>
<th>Area</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pentium 4</td>
<td>42,000,000</td>
<td>2000</td>
<td>Intel</td>
<td>180 nm</td>
<td></td>
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<tr>
<td>Atom</td>
<td>47,000,000</td>
<td>2008</td>
<td>Intel</td>
<td>45 nm</td>
<td></td>
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<tr>
<td>Barton</td>
<td>54,300,000</td>
<td>2003</td>
<td>AMD</td>
<td>130 nm</td>
<td></td>
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<tr>
<td>AMD K8</td>
<td>105,900,000</td>
<td>2003</td>
<td>AMD</td>
<td>130 nm</td>
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<tr>
<td>Itanium 2</td>
<td>220,000,000</td>
<td>2003</td>
<td>Intel</td>
<td>130 nm</td>
<td></td>
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<tr>
<td>Cell</td>
<td>241,000,000</td>
<td>2006</td>
<td>Sony/IBM/Toshiba</td>
<td>90 nm</td>
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<tr>
<td>Core 2 Duo</td>
<td>291,000,000</td>
<td>2006</td>
<td>Intel</td>
<td>65 nm</td>
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<tr>
<td>AMD K10</td>
<td>463,000,000[^1]</td>
<td>2007</td>
<td>AMD</td>
<td>65 nm</td>
<td></td>
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<tr>
<td>AMD K10</td>
<td>758,000,000[^1]</td>
<td>2008</td>
<td>AMD</td>
<td>45 nm</td>
<td></td>
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<tr>
<td>Itanium 2 with 9MB cache</td>
<td>592,000,000</td>
<td>2004</td>
<td>Intel</td>
<td>130 nm</td>
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<tr>
<td>Core i7 (Quad)</td>
<td>731,000,000</td>
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<td>Intel</td>
<td>45 nm</td>
<td>263 mm²</td>
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<tr>
<td>POWER6</td>
<td>789,000,000</td>
<td>2007</td>
<td>IBM</td>
<td>65 nm</td>
<td>341 mm²</td>
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<td>Six-Core Opteron 2400</td>
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<td>2009</td>
<td>AMD</td>
<td>45 nm</td>
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<td>Six-Core Core i7</td>
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<td>Intel</td>
<td>32 nm</td>
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<td>POWER7</td>
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<td>45 nm</td>
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<tr>
<td>z196[^2]</td>
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<td>IBM</td>
<td>45 nm</td>
<td>512 mm²</td>
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<tr>
<td>Dual-Core Itanium 2</td>
<td>1,700,000,000[^3]</td>
<td>2006</td>
<td>Intel</td>
<td>90 nm</td>
<td>596 mm²</td>
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<tr>
<td>Six-Core Xeon 7400</td>
<td>1,900,000,000</td>
<td>2008</td>
<td>Intel</td>
<td>45 nm</td>
<td></td>
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<tr>
<td>Quad-Core Itanium Tukwila</td>
<td>2,000,000,000[^4]</td>
<td>2010</td>
<td>Intel</td>
<td>65 nm</td>
<td></td>
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<tr>
<td>8-Core Xeon Nehalem-EX</td>
<td>2,300,000,000[^5]</td>
<td>2010</td>
<td>Intel</td>
<td>45 nm</td>
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Some Semiconductor Trends: Microprocessors

### GPUs

<table>
<thead>
<tr>
<th>Processor</th>
<th>Transistor count</th>
<th>Date of introduction</th>
<th>Manufacturer</th>
<th>Process</th>
<th>Area</th>
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<tr>
<td>G80</td>
<td>681,000,000</td>
<td>2006</td>
<td>NVIDIA</td>
<td>90 nm</td>
<td>480 mm²</td>
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<td>RV770</td>
<td>956,000,000[6]</td>
<td>2008</td>
<td>AMD</td>
<td>55 nm</td>
<td>260 mm²</td>
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<tr>
<td>RV850</td>
<td>1,040,000,000[7]</td>
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<td>AMD</td>
<td>40 nm</td>
<td>170 mm²</td>
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<td>GT200</td>
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<td>NVIDIA</td>
<td>55 nm</td>
<td>576 mm²</td>
</tr>
<tr>
<td>RV870</td>
<td>2,154,000,000[9]</td>
<td>2009</td>
<td>AMD</td>
<td>40 nm</td>
<td>334 mm²</td>
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<tr>
<td>GF100</td>
<td>3,000,000,000[10]</td>
<td>2010</td>
<td>NVIDIA</td>
<td>40 nm</td>
<td>529 mm²</td>
</tr>
</tbody>
</table>

### FPGA

<table>
<thead>
<tr>
<th>FPGA</th>
<th>Transistor count</th>
<th>Date of introduction</th>
<th>Manufacturer</th>
<th>Process</th>
<th>Area</th>
</tr>
</thead>
<tbody>
<tr>
<td>Virtex</td>
<td>~70,000,000</td>
<td>1997</td>
<td>Xilinx</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Virtex-E</td>
<td>~200,000,000</td>
<td>1998</td>
<td>Xilinx</td>
<td></td>
<td></td>
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<tr>
<td>Virtex-II</td>
<td>~350,000,000</td>
<td>2000</td>
<td>Xilinx</td>
<td>130 nm</td>
<td></td>
</tr>
<tr>
<td>Virtex-II PRO</td>
<td>~430,000,000</td>
<td>2002</td>
<td>Xilinx</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Virtex-4</td>
<td>1,000,000,000</td>
<td>2004</td>
<td>Xilinx</td>
<td>90 nm</td>
<td></td>
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<tr>
<td>Virtex-5</td>
<td>1,100,000,000[11]</td>
<td>2006</td>
<td>Xilinx</td>
<td>65 nm</td>
<td></td>
</tr>
<tr>
<td>Stratix IV</td>
<td>2,500,000,000[12]</td>
<td>2008</td>
<td>Altera</td>
<td>40 nm</td>
<td></td>
</tr>
</tbody>
</table>
How do things look today?

Quad-Core Intel® Core i7 Processor Up to 3.4GHz in 32nm CMOS, Power Dissipation: 95 watts
Some Semiconductor Trends: Microprocessors

Figure 1. Microprocessor complexity (transistor count) over time
Some Semiconductor Trends: Microprocessors

Figure 2. Microprocessor power consumption over time
Some Semiconductor Trends: Microprocessors

Figure 3. Microprocessor clock frequency over time
Some Semiconductor Trends: Microprocessors

Figure 4. Microprocessor core count over time

EE330, Spring 2014, Lecture #
Some Semiconductor Trends: Memory

Figure 7.1: Actual and predicted evolution of circuit complexity in DRAMs and microprocessors.

Physics of semiconductor devices By Jean-Pierre Colinge, Cynthia A. Colinge
Some Semiconductor Trends: Memory

**NAND Flash Memory:** Significant developments in NAND flash memory over the past few years, resulting in high-density, low-power, and low-cost storage solutions that are enabling the replacement of traditional hard-disk storage with solid-state disks (SSDs). Figure 5 shows the observed trend in NAND flash capacities presented at ISSCC in the past 12 years. Note that in 2010, the reduction in process feature sizes, coupled with advanced multi-level cell (MLC) techniques have yielded a 32Gb/chip capacity in a 32nm technology with 2b/cell operation.

**Figure 5. NAND Flash Memory Trends**
Some Semiconductor Trends: Data Rate

Figure 8. Data Rate Trend Chart
The Semiconductor Industry: Challenges

- Managing increasing device count
- Short lead time from conception to marketplace
- Process technology advances
- Device Performance Degradation
- Increasing variability
- Increasing pressure for cost reduction
- Power Dissipation
Is there an end in sight?

No, but the direction the industry will follow is not yet known. However, the role semiconductor technology plays on society will certainly increase dramatically!

Will engineers trained in this field become obsolete at mid-career?

Also, NO! Engineers trained in this field will naturally evolve to support the microelectronics technology of the future. Integrated Circuit designers are now being trained to efficiently manage enormous levels of complexity and any evolutionary technology will result in even larger and more complex systems with similar and expanded skills being required even if the details are different.
The Semiconductor Industry: Opportunities

◆ Will engineers trained in this field become obsolete at mid-career?

➢ There have been substantive changes in approaches every few years since 1965 and those changes will continue. Continuing education to track evolutionary and revolutionary changes in the field will be essential to remain productive in the field.

◆ What changes can we expect to see beyond the continued geometric growth in complexity (functional capability)?

➢ That will be determined by the creativity and marketing skills of those who become immersed in the technology. New “Gordon Moores”, “Bill Gates” and “Jim Dells” will evolve.
The Integrated Circuit (IC)

◆ What exactly is an electronic circuit?
   ➢ An electronic circuit is comprised of transistors along with some passive components (resistors, capacitors, and inductors) and maybe a few diodes connected together to perform a desired function → some form of processing of an electrical voltage or current

◆ Before the invention of the IC, every component was in its own separate chip and package, and wiring components (interconnects) was done externally to the components

◆ Even the simplest circuit would occupy a very large space → limits the complexity of the circuits we can build

◆ So What exactly is an Integrated Circuit (IC)?
   ➢ An IC enables us to implement all the transistors and a small number of passive components together on the same chip and package, including wiring (interconnects) → this process is called “integration”
The Integrated Circuit (IC)

- The impact of the IC on the electronics industry
  - Much more complicated circuits can be built with billions of transistors → Very Large Scale of Integration (VLSI)
  - Dramatic reduction in cost and size of electronic circuits

- This course will focus on understanding how transistors operate and on how they can be interconnected and possibly combined with a small number of passive components to form useful integrated circuits

- We will also study how transistors, diodes, and passive components are fabricated and connected together on a single chip using semiconductor fabrication processes
Computer Aided Design (CAD)
As the IC and the number of transistors within it become larger, how do we manage the design and verification process efficiently and with a low probability of error?

Computer Aided Design (CAD) tools and CAD-tool environment is critical for success today.

However, CAD toolsets only help the engineer, and it is highly unlikely that they will replace the design engineer.

Surprisingly, there is only a small number of VLSI CAD toolset vendors that dominate the market.
CAD Environment for IC Design

◆ An emphasis in this course will be placed on using CAD toolsets and CAD environment to support the design and verification process

◆ Typical Tool Flow
  ➢ See Chapter 14 of Text

◆ Laboratory Experiments in Course
VLSI Design Flow Summary: Analog

System Description

Circuit Design (Schematic)

SPICE Simulation

Layout/DRC...

DRC Error Report

Parasitic Extraction

LVS

LVS Error Report

Fabrication

Back annotated Schematic

Post-Layout Simulation
VLSI Design Flow Summary: Analog

1. System Description
2. Circuit Design (Schematic)
   - Schematic Editor
   - SPICE Simulation
3. Layout/DRC...
   - Assura DRC
   - Parasitic Extraction
4. Post-Layout Simulation
   - Spectre (or HSPICE)
5. Fabrication
   - Back annotated Schematic
6. LVS
   - Assura LVS
   - LVS Error Report
7. Cadence Virtuoso
   - Assura RCX
8. Simulation Results
   - DRC Error Report

Tools:
- Spectre (or HSPICE)
- Cadence
- Assura RCX
- Assura DRC
VLSI Design Flow Summary: Digital

System Description

Verilog Description

Verilog Simulation

Synthesis (Synopsys)

Place and Route (SoC Encounter)

--- DEF or GDS2 File

Simulate (Gate Level)

Gate-level Simulation

VHDL Simulation Results and And Comparison with System Specs.

Circuit Schematic (Cadence)

Connectivity Report and Show Routing to TA

LVS

Print Circuit Schematic

LVS Output File

Post-Layout Simulation

Fabrication

Back-Annotated Extraction

DRC

DRC Report

Extraction

Post-Layout Simulation

EE330, Spring 2014, Lecture #
VLSI Design Flow Summary: Digital

System Description

Verilog Description

Verilog Simulation

Synthesis

Place and Route (SoC Encounter)

--- DEF or GDS2 File ---

DRC

Back-Annotated Extraction

Post-Layout Simulation

Fabrication

DRC Report

Extraction

Connected Reports and Show Routing to TA

Circuit Schematic (Cadence)

LVS

LVS Output File

Post-Layout Simulation

Print Circuit Schematic

Gate-level Simulation

VHDL Simulation Results and And Comparison with System Spec.

Cadence SoC Encounter

Verilog XL

Synopsis

Simulate (Gate Level)
VLSI Design Flow Summary: Mixed-Signal

- System Description
- VHDL Description
- VHDL Simulation
- Synthesis (Synopsys)
- Simulate (Gate Level)
- Place and Route (Silicon Ensemble)
  --- DEF or GDS2 File ---
- DRC
  --- DRC Report ---
- Extraction
- Back-Annotated Extraction
- Post-Layout Simulation

The Digital Part

- VHDL Simulation Results and Comparison with System Specs.
- Gate-level Simulation
- Print Circuit Schematic
- Create Circuit Schematic
- LVS
  - Connectivity Report and Show Routing to TA
  - LVS Output File
  - Post-Layout Simulation
VLSI Design Flow Summary: Mixed-Signal

1. System Description
2. Circuit Design (Schematic)
3. SPICE Simulation
4. Layout/DRC
5. Extraction
7. Post-Layout Simulation
8. LVS
9. LVS Output File
10. Print Circuit Schematic

The Analog Part

DRC Report

Simulation Results

C

D
VLSI Design Flow Summary: Mixed-Signal

A → Layout Merge → Extraction → LVS/DRC → Fabrication

C → Analog-Digital Merger → LVS/DRC

D → Schematic Merge → LVS/DRC

B → Show Layout to TA → Post-Layout Simulation → Simulation Results
The Analog Design Flow is often used for small digital blocks or when particular structure or logic styles are used in digital systems.

The Analog Design Flow is also often used for small digital blocks within bigger analog blocks.

Variants of these flows are widely used and often personalized by a given company or for specific classes of circuits.
The Semiconductor Process

The Transistor, Reliability and Yield, Review of Basic Statistical Concepts, A Brief History
A MOS transistor is formed through the overlap between two different materials—Poly-silicon (Poly) and n-type or p-type silicon (Active, and sometimes called Diffusion). The two materials are implemented on two vertically spaced levels, where overlap does not mean intersection.
The Metal Oxide Semiconductor (MOS) Transistor

- Although the area of the transistor is the bounding region, its functional portion (the Channel) is only the overlap → the rest is necessary to be able to connect to the transistor.
- The geometric overlap is referred to as the Drawn Width (W) and Drawn Length (L) of the transistor.
The Metal Oxide Semiconductor (MOS) Transistor

- Although the area of the transistor is the bounding region, its functional portion (the Channel) is only the overlap → the rest is necessary to be able to connect to the transistor.
- The actual source and drain is actually at the edge.
The Metal Oxide Semiconductor (MOS) Transistor

- The Effective width and length of the transistor are generally smaller than Drawn Width and Length

![Diagram of MOS Transistor]

- Actual Source
- Actual Drain
- Gate
- Region of Interest (Channel)
- Effective Width: $W_{\text{eff}}$
- Effective Length: $L_{\text{eff}}$
The Feature Size

The Feature Size is the minimum lateral size a certain feature can be reliably implemented in a given fabrication process

- The minimum Width and Length of a transistor
- The minimum metal interconnect width
- The minimum spacing between metal interconnects
- Etc...
The Feature Size

- Usually the Feature Size is the same for many features in a given technology
- Often specified in terms of pitch
- Pitch is approximately equal to twice minimum feature size
### Feature Size Evolution

<table>
<thead>
<tr>
<th>Year</th>
<th>Feature Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mid 70's</td>
<td>25µ</td>
</tr>
<tr>
<td>2005</td>
<td>90nm</td>
</tr>
<tr>
<td>2010</td>
<td>20nm</td>
</tr>
<tr>
<td>2020</td>
<td>10nm</td>
</tr>
</tbody>
</table>

\[ 1\mu = 10^3 nm = 10^{-6} m = 10^4 \text{ Å} \]
Feature Size Evolution

◆ Size of Atoms and Molecules in Semiconductor Processes

Silicon:  
- Average Atom Spacing: 2.7 Å
- Lattice Constant: 5.4 Å

$\text{SiO}_2$:  
- Average Atom Spacing: 3.5 Å

Air:  
- Breakdown Voltage: 5 to 10 MV/cm = 5 to 10 mV/Å
- 20 KV/cm

◆ Physical size of atoms and molecules place fundamental limit on conventional scaling approaches
Technology Nomenclature

- Depending on the number of transistors implemented in a given IC
  - SSI → Small Scale of Integration → 1-100
  - MSI → Medium Scale of Integration → 100-10³
  - LSI → Large Scale of Integration → 10³-10⁵
  - VLSI → Very Large Scale of Integration → 10⁵-10⁶

- Any design in a process capable of incorporating a large number of devices is generally termed a VLSI design
Technology Nomenclature

- Depending on the number of transistors implemented in a given IC
  - SSI → Small Scale of Integration → 1-100
  - MSI → Medium Scale of Integration → 100-10^3
  - LSI → Large Scale of Integration → 10^3-10^5
  - VLSI → Very Large Scale of Integration → 10^5-10^6

- Any design in a process capable of incorporating a large number of devices is generally termed a VLSI design
The Die versus the Wafer

- The Die refers to the silicon area where a full design is implemented (this is what is inside the package of an IC).
- The Wafer is a large silicon disc that contains many copies of the same Die.
- God bless the invention of copy/paste!

A Wafer is 6 inches to 12 inches in diameter with a flat edge. A very large number of die can be produced if the die size is small.
Characterize the high-volume incremental costs of manufacturing integrated circuits

Example: Assume manufacturing cost of an 8” wafer in a 0.25µ process is $800. Determine the number of minimum-sized transistors that can be fabricated on this wafer and the cost per transistor. Neglect spacing and interconnect.

Solution:

\[
\begin{align*}
n_{\text{trans}} & \approx \frac{A_{\text{wafer}}}{A_{\text{trans}}} = \frac{\pi (4\text{in})^2}{(0.25\mu)^2} = 5.2E11 \\
C_{\text{trans}} &= \frac{C_{\text{wafer}}}{n_{\text{trans}}} = \frac{$800}{5.2E11} = $15.4E-9
\end{align*}
\]

Device count may be decreased by a factor of 10 or more if interconnect and spacing is included but even with this decrease, the cost per transistor is still very low!
Device and Die Cost

- From the previous example

\[ C_{\text{per unit area}} \approx \$2.5 / cm^2 \]

Example: If the die area of the 741 op amp is 1.8 mm\(^2\) (including bonding pads), determine the cost of the silicon needed to fabricate this op amp

\[ C_{741} = \$2.5 / cm^2 \times (1.8 mm^2) \approx \$0.05 \]

Actual integrated op amp will be dramatically less if bonding pads are not needed.

- The smaller a circuit is \(\rightarrow\) the more copies you can fabricate on a single wafer \(\rightarrow\) the cheaper the circuit is even if the fabrication cost of the wafer stays the same.

- This is why we love scaling \(\rightarrow\) although fabrication cost may increase, reduction in the cost of the IC can decrease.
Reliability and Yield

◆ The Feature Size is the minimum lateral size a certain feature can be **reliably** implemented in a given fabrication process → What does reliably actually mean?
Upon fabricating a very large number of copies of a given feature or function, what is the probability that these copies will actually turn out to have the intended feature or function, or within an acceptable error from the intended feature or function.

If \( P \) is the probability that a feature is “good”

\( n \) is the number of features on an IC

\( Y \) is the yield (probability that all features are simultaneously good)

\[
Y = P \times P \times P \ldots = P^n
\]

\[
P = e^{\frac{\log_e Y}{n}}
\]
Reliability and Yield

◆ How reliable does a given feature must be?
◆ Let’s say the number of features n=5E3
◆ Let’s say we would like our yield to be Y=0.9

\[ P = e^{\frac{\log_e Y}{n}} = e^{\frac{\log_e 0.9}{5E3}} = 0.999979 \]

◆ Is n=5E3 realistic? → Not really → n=5E9 is more like it!

\[ P = e^{\frac{\log_e Y}{n}} = e^{\frac{\log_e 0.9}{5E9}} = 0.999999999979 \]

◆ Extremely high reliability must be achieved per feature to obtain acceptable overall yields
◆ Yield dramatically affect Die and Device Cost
Dust particles and other undesirable processes cause defects → These defects in manufacturing cause yield loss
Yield Issues: Hard Faults

- Defects in processing cause yield loss
- The probability of a defect causing a circuit failure increases with die area
- The circuit failures associated with these defects are termed Hard Faults
- This is the major factor limiting the size of die in integrated circuits
- Several different models have been proposed to model the hard faults
Yield Issues: Hard Fault Models

\[ Y_H = e^{-Ad} \]

- \( Y_H \) is the probability that the die does not have a hard fault
- \( A \) is the die area
- \( d \) is the defect density (typically \( 1\text{cm}^{-2} < d < 2\text{cm}^{-2} \))

- Industry often closely guards the value of \( d \) for their process
- Other models, which may be better, have the same general functional form
Yield Issues: Soft Faults

- Random parametric variations in a process can also cause circuit failure or cause circuits to not meet desired performance specifications (this is of particular concern in analog and mixed-signal circuits)

- The circuit failures associated with these parametric variations are termed Soft Faults

- Decreases with area, judicious layout and routing, and clever circuit design techniques can reduce the effects of soft faults
Yield Issues: Soft Fault Models

- Soft fault models often depend on design and application.
- Often the standard deviation of a parameter depends on the reciprocal of the square root of the parameter’s sensitive area.

\[ \sigma = \frac{\rho}{\sqrt{A_k}} \]

\( \rho \) is a constant dependent upon the architecture and the process.

\( A_k \) is the area of the parameter’s sensitive area.
Yield Issues: Soft Fault Models

\[ P_{SOFT} = \int_{X_{MIN}}^{X_{MAX}} f(x) \, dx \]

- \( P_{SOFT} \) is the soft fault yield
- \( f(x) \) is the probability density function of the parameter of interest
- \( X_{MIN} \) and \( X_{MAX} \) define the acceptable range of the parameter of interest

\[ \int_{X_{MIN}}^{X_{MAX}} f(x) \, dx \]

Some circuits may have several parameters that must meet performance requirements.
Yield Issues: Soft Fault Models

If there are $k$ parameters that must meet certain parametric performance requirements and if the random variables characterizing these parameters are uncorrelated, then the soft yield is given by

$$Y_S = \prod_{j=1}^{k} P_{SOFT_j}$$
If both hard and soft faults affect the yield of a circuit, the overall yield is given by the expression

\[ Y = Y_H Y_S \]
Yield Issues: Yield and Die Cost

- The overall yield can dramatically affect Die cost
- The manufacturing cost per “good” Die is given by

\[
C_{\text{Good}} = \frac{C_{\text{FabDie}}}{Y}
\]

where \(C_{\text{FabDie}}\) is the manufacturing costs of a fab die and \(Y\) is the yield

- There are other costs that must ultimately be included such as testing costs, engineering costs, etc.
- Let’s take an example!
Yield Issues: Yield and Die Cost

- Assume a die has no soft fault vulnerability, a die area of 1cm$^2$, and a process that has a defect density of 1.5cm$^{-2}$
- Determine the hard yield
- Determine the manufacturing cost per “good” Die if 8-inch wafer is used and if the cost of the wafer is $1200

\[
Y_H = e^{-Ad} = e^{-1\text{cm}^2 \times 1.5\text{cm}^{-2}} = 0.22
\]

\[
C_{\text{FabDie}} = \frac{C_{\text{Wafer}}}{A_{\text{Wafer}}} A_{\text{Die}} = \frac{$1200}{\pi (4\text{in})^2} 1\text{cm}^2 = $3.82
\]

\[
C_{\text{Good}} = \frac{C_{\text{FabDie}}}{Y} = \frac{$3.82}{0.22} = $17.37
\]
Review of Basic Concepts of Statistics

◆ Statistics govern what really happens throughout much of the engineering field!

◆ Statistics characterize what WILL happen in many processes → You MUST know the basics of it whether you like it or not!

◆ For instance, you must rely on it to determine yield and subsequently cost → If you don’t use it, you can’t find out if your investment is worthwhile
Review of Basic Concepts of Statistics

Assume $x$ is a random variable of interest

$f(x) = \text{Probability Density Function (PDF)}$ for $x$

$$\int_{-\infty}^{\infty} f(x) \, dx = 1$$

$F(x) = \text{Cumulative Density Function (CDF)}$ for $x$

$$F(X_1) = \int_{-\infty}^{x_1} f(x) \, dx$$

$$0 \leq F(x) \leq 1 \quad \frac{\partial F(x)}{\partial x} \geq 0$$
Review of Basic Concepts of Statistics

\[ f(x) = \text{Probability Density Function (PDF) for } x \]

\[ F(x) = \text{Cumulative Density Function (CDF) for } x \]

\[
P\{x \leq x_1\} = \int_{-\infty}^{x_1} f(x) \, dx
\]

\[
P\{x \leq X_1\} = F(X_1)
\]
Review of Basic Concepts of Statistics

\[ f(x) = \text{Probability Density Function (PDF) for } x \]
\[ F(x) = \text{Cumulative Density Function (CDF) for } x \]

\[ P\{X_1 \leq x \leq X_2\} = \int_{X_1}^{X_2} f(x) \, dx \]
\[ P\{X_1 \leq x \leq X_2\} = F(X_2) - F(X_1) \]
How to we obtain the PDF of a given random variable?

- Most parameters we deal with in microelectronic circuits have what we call a “Normal distribution”, which is also called “Gaussian distribution”.
- Experimental observations confirm that and provide close agreement between theoretical and experimental results.

What exactly is a Normal distribution?
What exactly is a Normal distribution?

- The PDF of a Normal distribution is fully characterized and tabulated through its Mean ($\mu$) and Standard Deviation ($\sigma$).
- A Normal distribution is referred to as $N(\mu, \sigma)$.
Review of Basic Concepts of Statistics

What exactly is a Normal distribution?

- A Normal distribution is referred to as $N(\mu, \sigma)$

![Normal distribution diagram]

- 68% of the data falls within one standard deviation of the mean ($\mu \pm \sigma$).
- 95% of the data falls within two standard deviations of the mean ($\mu \pm 2\sigma$).
- 99.7% of the data falls within three standard deviations of the mean ($\mu \pm 3\sigma$).
Review of Basic Concepts of Statistics

◆ A Normal distribution has some interesting features

Theorem 1: If the random variable $x$ is normally distributed with mean $\mu$ and standard deviation $\sigma$, then $y = \frac{x - \mu}{\sigma}$ is also a random variable that is normally distributed with mean 0 and standard deviation of 1.

◆ Why is that an important feature?

- Because it means I don’t have to tabulate every single PDF just because it has a different $\mu$ and $\sigma$
- As long as the distribution is normal, I can convert it to a PDF with Zero mean and unity Sigma, compute my probability, then scale it back to obtain the actual probability for the specific PDF I want → How?
We know the following

If $x$ is a Normal (Gaussian) random variable with mean $\mu$ and standard deviation $\sigma$, then the probability that $x$ is between $x_1$ and $x_2$ is given by

$$p = \int_{x_1}^{x_2} f(x) \, dx$$
Review of Basic Concepts of Statistics

- If \(f(x)\) is the PDF of a Normal distribution with mean \(\mu\) and standard deviation \(\sigma\), while \(f_n(x)\) is the PDF of a Normal distribution with Zero mean and unity standard deviation, then we can show that

\[
p = \int_{x_1}^{x_2} f(x) \, dx = \int_{x_{1n}}^{x_{2n}} f_n(x) \, dx
\]

where \(x_{1n} = \frac{x_1 - \mu}{\sigma}\) and \(x_{2n} = \frac{x_2 - \mu}{\sigma}\)
Review of Basic Concepts of Statistics

- We also Know that

\[ p = \int_{x_1}^{x_2} f(x) \, dx = F(x_2) - F(x_1) \]

- And we can show that

\[ p = \int_{x_{1n}}^{x_{2n}} f_n(x) \, dx = F_n(x_{2n}) - F_n(x_{1n}) \]

- Where \( F(x) \) and \( F_n(x) \) are the CDF of both distributions
Review of Basic Concepts of Statistics

In many electronic circuits, the random variables of interest are 0 mean Gaussian and the probabilities of interest are characterized by a region defined by the magnitude of the random variable. The variable is symmetric around zero.

\[
p = \int_{-x_{1n}}^{x_{1n}} f_n(x) \, dx = F_n(x_{1n}) - F_n(-x_{1n}) = 2F_n(x_{1n}) - 1
\]
Tables of the CDF of the N(0,1) random variable are readily available. It is also available in Matlab, Excel, and a host of other sources.

![Probability Content from -oo to Z table](http://www.math.unb.ca/~knight/utility/NormTble.htm)
Example: Determine the probability that the N(0,1) random variable has magnitude less than 2.6

\[ p = 2F_n(2.6) - 1 \]

From the table of the CDF, \( F_n(2.6) = 0.9953 \) so \( p = 0.9906 \)
Review of Basic Concepts of Statistics

Example: Determine the soft yield of an operational amplifier that has an offset voltage requirement of 5mV if the standard deviation of the offset voltage is 2.5mV and the mean is 0V.

\[ y = \frac{x-0}{2.5} \]

\[ p = \int_{-2}^{2} f_N(x) \, dx = F_N(2) - F_N(-2) = 2F_N(2) - 1 \]

\[ p = 2F_N(2) - 1 = 2 \times 0.9772 - 1 = 0.9544 \]
History 101

- 1925, 1935 → The concept of the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) Transistor Proposed (Lilienfield and Heil)
- 1947 → The Bipolar Junction Transistor (BJT) conceived and experimentally verified (Bardeen, Bratin and Shockley of Bell Labs)
- 1959 → Jack Kilby from Texas Instruments, and Bob Noyce from Fairchild invent the Integrated Circuit
- 1963 → Wanless from Fairchild experimentally verifies the MOS Gate
1926 - Field Effect Semiconductor Device Concepts Patented

Julius Lilienfeld files a patent describing a three-electrode amplifying device based on the semiconducting properties of copper sulfide. Attempts to build such a device continue through the 1930s.

Polish-American physicist and inventor Julius E. Lilienfeld filed a patent in 1926, "Method and Apparatus for Controlling Electric Currents," in which he proposed a three-electrode structure using copper-sulfide semiconductor material. Today this device would be called a field-effect transistor. While working at Cambridge University in 1934, German electrical engineer and inventor Oskar Heil filed a patent on controlling current flow in a semiconductor via capacitive coupling at an electrode - essentially a field-effect transistor. Although both patents were granted, no records exist to prove that Heil or Lilienfeld actually constructed functioning devices.

Heil, O. "Improvements in or relating to electrical amplifiers and other control arrangements and devices," British Patent No. 439, 457 (Filed March 5, 1935. Issued December 6, 1935).
Patented Jan. 28, 1930

UNITED STATES PATENT OFFICE

JULIUS EDGAR LILIENTHAL, OF BROOKLYN, NEW YORK

METHOD AND APPARATUS FOR CONTROLLING ELECTRIC CURRENTS

Application filed October 8, 1926, Serial No. 140,363, and in Canada October 22, 1925.

Jan. 28, 1930. J. E. LILIENTHAL 1,745,175

METHOD AND APPARATUS FOR CONTROLLING ELECTRIC CURRENTS

Filed Oct. 8, 1926

Fig. 1.
March 7, 1933.

J. E. LILIENFELD

DEVICES FOR CONTROLLING ELECTRIC CURRENT

Filed March 28, 1928

1,900,018

3 Sheets-Sheet 1

Fig. 1.

12 Copper Sulfide
11 Aluminum Oxide
10 Aluminum

Fig. 2.

12 Copper Sulfide
11 Aluminum Oxide
10 Aluminum
From the group at Bell Labs

“We have called it the transistor, T-R-A-N-S-I-S-T-O-R, because it is resistor or semiconductor device which can amplify electrical signals as they are transferred through it from input to output terminals. It is, if you will, the electrical equivalent of a vacuum tube amplifier. But there the similarity ceases. It has no vacuum, no filament, no glass tube. It is composed entirely of cold, solid substances.”
History 101

William Shockley

http://www.time.com/time/time100/scientist/profile/shockley03.html
William Shockley

He fathered the transistor and brought the silicon to Silicon Valley but is remembered by many only for his noxious racial views

By GORDON MOORE

The transistor was born just before Christmas 1947 when John Bardeen and Walter Brattain, two scientists working for William Shockley at Bell Telephone Laboratories in Murray Hill, N.J., observed that when electrical signals were applied to contacts on a crystal of germanium, the output power was larger than the input. Shockley was not present at that first observation. And though he fathered the discovery in the same way Einstein fathered the atom bomb, by advancing the idea and pointing the way, he felt left out of the momentous occasion.

Shockley, a very competitive and sometimes infuriating man, was determined to make his imprint on the discovery. He searched for an explanation of the effect from what was then known of the quantum physics of semiconductors. In a remarkable series of insights made over a few short weeks, he greatly extended the understanding of semiconductor materials and developed the underlying theory of another, much more robust amplifying device — a kind of sandwich made of a crystal with varying impurities added, which came to be known as the junction transistor. By 1951 Shockley's co-workers made his semiconductor sandwich and demonstrated that it behaved much as his theory had predicted.
William Shockley
He fathered the transistor and brought the silicon to Silicon Valley but is remembered by many only for his noxious racial views

By GORDON MOORE

Not content with his lot at Bell Labs, Shockley set out to capitalize on his invention. In doing so, he played a key role in the industrial development of the region at the base of the San Francisco Peninsula. It was Shockley who brought the silicon to Silicon Valley.

In February 1956, with financing from Beckman Instruments Inc., he founded Shockley Semiconductor Laboratory with the goal of developing and producing a silicon transistor. He chose to establish this start-up near Palo Alto, where he had grown up and where his mother still lived. He set up operations in a storefront — little more than a Quonset hut — and hired a group of young scientists (I was one of them) to develop the necessary technology. By the spring of 1956 he had a small staff in place and was beginning to undertake research and development.

This new company, financed by Fairchild Camera & Instrument Corp., became the mother organization for several dozen new companies in Silicon Valley. Nearly all the scores of companies that are or have been active in semiconductor technology can trace the technical lineage of their founders back through Fairchild to the Shockley Semiconductor Laboratory. Unintentionally, Shockley contributed to one of the most spectacular and successful industry expansions in history.
William Shockley

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Editor's note:

In 1963 Shockley left the electronics industry and accepted an appointment at Stanford. There he became interested in the origins of human intelligence. Although he had no formal training in genetics or psychology, he began to formulate a theory of what he called dysgenics. Using data from the U.S. Army’s crude pre-induction IQ tests, he concluded that African Americans were inherently less intelligent than Caucasians — an analysis that stirred wide controversy among laymen and experts in the field alike.

(Fairchild was formed in 1957 – Moore and Noyce were 2 or 8 co-founders)
United States Patent

Kilby

[54] SEMICONDUCTOR DEVICE

[72] Inventor: Jack St. Clair Kilby, Dallas, Tex.

[73] Assignee: Texas Instruments Incorporated, Dallas, Tex.

[22] Filed: June 29, 1963

[21] Appl. No.: 169,797

Related U.S. Application Data


[51] Int. Cl. .................................. H01L 19/00

[58] Field of Search ....................... 317/234, 235, 101, 231

[56] References Cited

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Primary Examiner—James D. Kallam

Attorney—James O. Dixon, Andrew M. Hansell, Robert C.

Paterson and Stevens, Davis, Miller and Mosher

EXEMPLARY CLAIM

1. A semiconductor device comprising:

a. a wafer of semiconductor material having two major faces;

b. said wafer being so shaped as to define a plurality of regions within said wafer and adjacent to one of said major faces;

c. at least some of said regions being electrically isolated within said wafer from others of said regions;

d. said regions having at least one portion thereof extending to said one major face;

e. at least some of said portions having selected locations on said one major face for electrical contact to said region;

f. an insulating material on said one major face of the wafer excluding at least said selected locations;

g. at least one electrically conductive area in contact with said insulating material and spaced from said wafer thereby;

h. said electrically conductive area being disposed in cooperative relationship with respect to a selected one of said isolated regions so as to provide the electrical function of a discrete electrical circuit component; and

i. a plurality of metallic interconnections providing electrically conductive paths between said selected locations on different ones of said regions and between another selected one of said locations and said electrically conductive area.

4 Claims, 33 Drawing Figures

EE330, Spring 2014, Lecture #
History 101

Jack Kilby
There are few men whose insights and professional accomplishments have changed the world. Jack Kilby is one of these men. His invention of the monolithic integrated circuit - the microchip - some 45 years ago at Texas Instruments (TI) laid the conceptual and technical foundation for the entire field of modern microelectronics. It was this breakthrough that made possible the sophisticated high-speed computers and large-capacity semiconductor memories of today's information age.

Mr. Kilby grew up in Great Bend, Kansas. With B.S. and M.S. degrees in electrical engineering from the Universities of Illinois and Wisconsin respectively, he began his career in 1947 with the Centralab Division of Globe Union Inc. in Milwaukee, developing ceramic-base, silk-screen circuits for consumer electronic products.

In 1958, he joined TI in Dallas. During the summer of that year working with borrowed and improvised equipment, he conceived and built the first electronic circuit in which all of the components, both active and passive, were fabricated in a single piece of semiconductor material half the size of a paper clip. The successful laboratory demonstration of that first simple microchip on September 12, 1958, made history.

Jack Kilby went on to pioneer military, industrial, and commercial applications of microchip technology. He headed teams that built both the first military system and the first computer incorporating integrated circuits. He later co-invented both the hand-held calculator and the thermal printer that was used in portable data terminals.
History 101

Robert Noyce
Robert Norton Noyce was born December 12, 1927 in Burlington, Iowa. A noted visionary and natural leader, Robert Noyce helped to create a new industry when he developed the technology that would eventually become the microchip. Noted as one of the original computer entrepreneurs, he founded two companies that would largely shape today’s computer industry—Fairchild Semiconductor and Intel.

Bob Noyce's nickname was the "Mayor of Silicon Valley." He was one of the very first scientists to work in the area -- long before the stretch of California had earned the Silicon name -- and he ran two of the companies that had the greatest impact on the silicon industry: Fairchild Semiconductor and Intel. He also invented the integrated chip, one of the stepping stones along the way to the microprocessors in today's computers.

Noyce, the son of a preacher, grew up in Grinnell, Iowa. He was a physics major at Grinnell College, and exhibited while there an almost baffling amount of confidence. He was always the leader of the crowd. This could turn against him occasionally -- the local farmers didn't approve of him and weren't likely to forgive quickly when he did something like steal a pig for a college luau. The prank nearly got Noyce expelled, even though the only reason the farmer knew about it was because Noyce had confessed and offered to pay for it.

While in college, Noyce's physics professor Grant Gale got hold of two of the very first transistors ever to come out of Bell Labs. Gale showed them off to his class and Noyce was hooked. The field was young, though, so when Noyce went to MIT in 1948 for his Ph.D., he found he knew more about transistors than many of his professors.
After a brief stint making transistors for the electronics firm Philco, Noyce decided he wanted to work at Shockley Semiconductor. In a single day, he flew with his wife and two kids to California, bought a house, and went to visit Shockley to ask for a job -- in that order.

As it was, Shockley and Noyce's scientific vision -- and egos -- clashed. When seven of the young researchers at Shockley semiconductor got together to consider leaving the company, they realized they needed a leader. All seven thought Noyce, aged 29 but full of confidence, was the natural choice. So Noyce became the eighth in the group that left Shockley in 1957 and founded Fairchild Semiconductor.

Noyce was the general manager of the company and while there invented the integrated chip -- a chip of silicon with many transistors all etched into it at once. Fairchild Semiconductor filed a patent for a semiconductor integrated circuit based on the planar process on July 30, 1959. That was the first time he revolutionized the semiconductor industry. He stayed with Fairchild until 1968, when he left with Gordon Moore to found Intel. At Intel he oversaw Ted Hoff's invention of the microprocessor -- that was his second revolution.

At both companies, Noyce introduced a very casual working atmosphere, the kind of atmosphere that has become a cultural stereotype of how California companies work. But along with that open atmosphere came responsibility. Noyce learned from Shockley's mistakes and he gave his young, bright employees phenomenal room to accomplish what they wished, in many ways defining the Silicon Valley working style was his third revolution.
History 101

- 1971 → Intel Introduces 4004 microprocessor (2300 transistors, 10u process)
The Metal Oxide Semiconductor (MOS) Transistor

The Ideal Switch Level View
Modelling of Electronic Devices

◆ Each electronic device has corresponding models that can be used to describe its behavior

◆ These models can vary depending on the desired
  - Complexity
  - Accuracy
  - Insight
  - Application

◆ It is wise to use the simplest model that can provide acceptable results for any given application
The MOS Transistor: Qualitative Discussion

- There are two types of MOS transistors → n-channel and p-channel
- In an n-channel transistor, the current is conducted by electrons, while in a p-channel it is conducted by holes
- The transistor is a complicated device and can operate in many different modes, and will have unique behavior in each mode
- Each mode will have its unique model that describes its behavior
- We will gradually go through all the different modes and discover how the transistor can be used to build useful circuits
The MOS Transistor: n-Channel

Cross-Sectional View

Top View

Complete Symmetry in construction between Drain and Source

Designer always works with top view

Source
Gate
Drain

Bulk

n-channel MOSFET

n-type
n+-type
p-type
p+-type
SiO$_2$ (insulator)
POLY (conductor)

Symbol

Drain
Gate
Source

Designer always works with top view
The MOS Transistor: n-Channel

**Behavioral Description of Basic Operation**

- If $V_{GS}$ is large, short circuit exists between drain and source.
- If $V_{GS}$ is small (near zero), open circuit exists between drain and source.

![Diagram of n-channel MOSFET](image-url)
The MOS Transistor: n-Channel

Equivalent Circuit for n-channel MOSFET

- Source assumed to be connected to ground
- $G=0$ means the gate voltage is close to ground
- $G=1$ means the gate voltage is close to $V_{DD}$

This is the first model we have for the n-channel MOSFET → An Ideal Switch!
The MOS Transistor: n-Channel

- **Equivalent Circuit for n-channel MOSFET → An Ideal Switch**

- **Mathematically**

\[
I_D = 0 \quad \text{if } V_G \text{ is low } (V_{GSn} \text{ is small}) \rightarrow \text{The Switch is off}
\]
\[
V_{DS} = 0 \quad \text{if } V_G \text{ is high } (V_{GSn} \text{ is large}) \rightarrow \text{The Switch is on}
\]

When the switch is off, it behaves like an open circuit (infinite resistance)
When the switch is on it behaves like a short circuit (zero resistance)
The MOS Transistor: p-Channel

Complete Symmetry in construction between Drain and Source
The MOS Transistor: p-Channel

Behavioral Description of Basic Operation

- If $V_{GS}$ is large (negative), short circuit exists between drain and source $\rightarrow$ Large negative $V_{GS}$ is the same as large positive $V_{SG}$
- If $V_{GS}$ is small (near zero), open circuit exists between drain and source

p-channel MOSFET
The MOS Transistor: p-Channel

Equivalent Circuit for p-channel MOSFET

- Source assumed to be connected to $V_{DD}$
- $G=0$ means the gate voltage is close to ground
- $G=1$ means the gate voltage is close to $V_{DD}$

This is the first model we have for the p-channel MOSFET → A Complementary Ideal Switch!
The MOS Transistor: p-Channel

- **Equivalent Circuit for** p-channel **MOSFET → A Complementary Ideal Switch**

- **Mathematically**

  - $I_D = 0$ if $V_G$ is high (|$V_{GSp}$| is small, $V_{SGp}$ is small) → The Switch is off
  - $V_{DS} = 0$ if $V_G$ is low (|$V_{GSp}$| is large, $V_{SGp}$ is large) → The Switch is on

When the switch is off, it behaves like an open circuit (infinite resistance)

When the switch is on, it behaves like a short circuit (zero resistance)
The MOS Transistor: Comparison

Gate

Drain

Source

G = 0

G = 1

D

S

G = 0

G = 1

S

D
The MOS Transistor: Summary

- Models for the n-channel and p-channel MOS devices have been developed
  - Termed the ideal switch-level model
  - Several other models will be developed later
  - Invariably use simplest model that is justifiable
  - Will introduce better models only when needed

- Symbols have been introduced for the two basic transistors
  - Other symbols will be introduced later
Basic Logic Circuits

An Application to the MOS Transistor
Basic Logic Circuits

- So the MOS transistor can be used as an ideal switch, how is that useful?

**Logic Circuits!!**

- We will present a brief description of logic circuits based upon simple models and qualitative description of processes
- We will discuss process technology needed to develop better models
- We will provide more in-depth discussion of logic circuits based upon better device models
Boolean versus Continuous Notation

- Voltage Axis is Continuous between 0V and $V_{DD}$, while Boolean axis is discrete with only two points.

- Most logic circuits characterized by the relationship between the Boolean input/output variables though these correspond to voltage ranges on the continuous voltage axis.
From now on, and for logic circuits purposes

- A signal with a voltage level close to $V_{DD}$, will be referred to as logic “high” or simply “1”
- A signal with a voltage level close to Ground, will be referred to as logic “low” or simply “0”
- Note that “1” and “0” in this context do not describe actual voltage, but logic levels
The Boolean Inverter

- A Boolean Inverter is a logic gate that receives a Boolean input and produces an inverted Boolean output.
- If we have two ideal switches, we can implement it as follows:
  - The bottom switch should turn on when the input is high ("1") → so it must be a Switch.
  - The top switch should turn off when the input is high ("1") → so it must be a complementary Switch.

![Diagram of Boolean Inverter](image)
A Boolean Inverter is a logic gate that receives a Boolean input and produces an inverted Boolean output.

We can leverage the MOS transistor to implement the switches.
The Boolean Inverter

- This is what is called a Complementary MOS (CMOS) Inverter → it is not the only way to do it, but the most famous

Truth Table

<table>
<thead>
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A Boolean NOR is a logic gate that receives two Boolean inputs and produces a high (“1”) Boolean output only if the two inputs are low (“0”) → otherwise it should produce a low (“0”) Boolean output.

If we have 4 ideal switches, we can implement it as follows.
A Boolean NOR is a logic gate that receives two Boolean inputs and produces a high ("1") Boolean output only if the two inputs are low ("0") → otherwise it should produce a low ("0") Boolean output.

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The Boolean NOR

- A Boolean NOR is a logic gate that receives two Boolean inputs and produces a high (“1”) Boolean output only if the two inputs are low (“0”) → otherwise it should produce a low (“0”) Boolean output.
- If we have 4 ideal switches, we can implement it as follows.
A Boolean NOR is a logic gate that receives two Boolean inputs and produces a high (“1”) Boolean output only if the two inputs are low (“0”) → otherwise it should produce a low (“0”) Boolean output.

If we have 4 ideal switches, we can implement it as follows.
The Boolean NOR

◆ This is what is called a CMOS NOR Gate → it is not the only way to do it, but the most famous

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The Boolean NAND

- A Boolean NAND is a logic gate that receives two Boolean inputs and produces a low ("0") Boolean output only if the two inputs are high ("1") → otherwise it should produce a high ("1") Boolean output.
- If we have 4 ideal switches, we can implement it as follows.

<table>
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The NAND and NOR gates can be expanded to more than two inputs.

- n-input NOR gate
- n-input NAND gate
Logic Circuits: Summary

◆ Many logic functions can be implemented using a combination of the previous 3 logic gates we discussed

◆ Logic circuits that are implemented by interconnecting multi-input NAND and NOR gates are referred to as “Static CMOS Logic”

◆ Since the set of NAND gates is complete, any combinational logic function can be realized with only NAND gates

◆ Since the set NOR gates is complete, any combinational logic function can be realized with only NOR gates

◆ Many logic functions are realized with “Static CMOS Logic” and this is probably the dominant design style used today!

◆ Other methods for designing logic circuits exist

◆ Insight will be provided on how other logic circuits evolve
How many transistors are required to realize the following logic function in a basic CMOS process if static NAND and NOR gates are used? Assume A, B and C are available.

\[ F = A \cdot \overline{B} + \overline{A} \cdot C \]
How many transistors are required to realize the following logic function in a basic CMOS process if static NAND and NOR gates are used? Assume A, B and C are available.

\[ F = A \cdot \overline{B} + \overline{A} \cdot C \]

**One Solution**

20 transistors and 5 levels of logic
How many transistors are required to realize the following logic function in a basic CMOS process if static NAND and NOR gates are used? Assume A, B and C are available

$$F = \overline{A} \cdot \overline{B} + \overline{A} \cdot C$$

A second Solution → From basic Boolean Manipulations

$$F = \overline{A} + \overline{B} + \overline{A} \cdot C = \overline{A} + B + \overline{A} \cdot C$$

$$F = \overline{A} \cdot (1 + C) + B = \overline{A} + B$$

8 transistors and 3 levels of logic
Static Logic Circuits: Example 1

◆ How many transistors are required to realize the following logic function in a basic CMOS process if static NAND and NOR gates are used? Assume A, B and C are available

\[ F = \overline{A} \cdot \overline{B} + \overline{A} \cdot \overline{C} \]

◆ A third Solution → From basic Boolean Manipulations

\[ F = \overline{A} \cdot (1 + C) + B = \overline{A} + B \]

\[ F = \overline{A} + B = A \cdot \overline{B} \]

6 transistors and 2 levels of logic
How many transistors are required to realize the following logic function in a basic CMOS process if static NAND, NOR, and Inverter gates are used? Assume A, B, C and D are available.

\[ Y = (A \cdot B) + (C \cdot D) \]

Standard static CMOS implementation

3 levels of Logic
16 Transistors if Basic CMOS Gates are Used
Static Logic Circuits: Example 3

- **The XOR function → A widely used 2-input CMOS gate**
  \[ Y = A \oplus B \]

- **Standard static CMOS implementation**
  \[ Y = A \overline{B} + \overline{A}B \]

- 22 transistors and 5 levels of logic
  Too many devices and logic levels

- **Why is the device count and the number of logic level important?**
  - Implementation size
  - Propagation delay
Can a Boolean function be implemented with less number of transistors and logic levels if we don’t rely on standard NAND, NOR, and Inverter gates?

Let’s reconsider how these gates are implemented to start with.
Static Logic Circuits: PUN and PDN Logic

- The main observation is that there is always a Pull-UP Network (PUN) and a Pull-Down Network (PDN)
- There are 4 characteristics to static CMOS gates
  - PUN comprised of p-channel devices
  - PDN comprised of n-channel devices
  - One and only one of these networks is conducting at the same time
  - One of the two networks is always conducting
  - Rail to rail logic swings
  - Zero static power dissipation in both Y=1 and Y=0 states
As a result of the previous characteristics

The PUN and the PDN must have “complementary” structures. If n-channel devices are connected in series in the PDN, there must be corresponding p-channel devices connected in parallel and vice versa.

The inversion of the logic function is implemented in the PDN such that an “And” correspond to a series connection between devices, and an “OR” correspond to a parallel connection between devices.
Let’s consider the multi-input NOR gate
Static Logic Circuits: PUN and PDN Logic

Let’s consider the multi-input NAND gate
Static Logic Circuits: Complex Gates

- The concept can be expanded to more complicated logic functions

- Complex Gate Design procedure
  - Express $\bar{Y}$ as either SOP or POS form
  - Implement $\bar{Y}$ in the PDN
  - Implement $Y$ in the PUN (must complement the input variables since p-channel devices are used)
Static Logic Circuits: Complex Gates

Example

\[ Y = \overline{(A \cdot B)} + (C \cdot D) \]

\[ \overline{Y} = (A \cdot B) + (C \cdot D) \]

8 transistors and 1 logic level

16 Transistors and 3 logic levels
Example → The XOR function → $\bar{Y}$ is expressed as POS

$Y = A \oplus B = AB + \bar{A}\bar{B}$

$\bar{Y} = (\bar{A}B + \bar{A}\bar{B}) = \bar{A}\bar{B} \cdot \bar{A}\bar{B} = (\bar{A} + B) \cdot (A + \bar{B})$

Here $\bar{Y}$ is expressed as POS
Static Logic Circuits: Complex Gates

Example → The XOR function → $\bar{Y}$ is expressed as POS

$Y = A\overline{B} + \overline{A}B$

$\bar{Y} = (\overline{A+B}) \cdot (A+B)$

12 transistors and 2 levels of logic

Notice a significant reduction in the number of transistors required compared to standard implementation (22 transistors and 5 levels of logic)
Example \( \rightarrow \) The XOR function \( \rightarrow \bar{Y} \) is expressed as SOP

\[
Y = A \oplus B = AB + \bar{A}B
\]

\[
Y = (\bar{A}+B) \cdot (A+B) = (\bar{A} \cdot (A+B)) + (B \cdot (A+B))
\]

\[
= (\bar{A} \cdot \bar{B}) + (A \cdot B)
\]

You will still end up with the same number of transistors and logic levels.
Complex Logic Gates implement logic functions and can result in significant reduction in transistor count and levels of logic for realizing same function when compared to standard static CMOS implementations.

Termed a “Complex Logic Gate” implementation.

Some authors term this a “Compound Gate”
Pass Transistor Logic

- Standard static logic as well as complex logic gates require more complexity in order to implement basic non-inverting logic functions.

\[ Y = A \cdot B \]

6 transistors and 2 logic levels
Consider the simple AND function

\[ Y = A \cdot B \]

Requires only 2 transistors rather than 6 for a standard CMOS gate (and a resistor)
Pass Transistor Logic

- Consider the simple AND function → Even simpler pass transistor logic implementations are possible

\[ Y = A \cdot B \]

- Requires only 1 transistor and a resistor
Pass Transistor Logic

◆ Consider the XOR function

\[ Y = A \oplus B \]

◆ Requires only 6 transistors and 1 resistor, with two levels of logic
Consider the XOR function → eliminating the inverters is possible

\[ Y = A \oplus B \]

Requires only 2 transistors and 1 resistor, with 1 level of logic
Pass Transistor Logic

- Pass transistor logic is actually commonly used
- It offers significant reductions in complexity for some functions (particularly non-inverting)

- But life can’t be so good → There is always a caveat
  - The resistor may require more area than several hundred or even several thousand transistors
  - Signal levels may not go to VDD or to 0V
  - Static power dissipation may not be zero
  - Signals may degrade unacceptably if multiple gates are cascaded

- The “resistor” is often implemented with a transistor to reduce area but signal swing and power dissipation problems still persist
Logic Design Styles: A Summary

- Several different logic design styles are often used throughout a given design (3 considered thus far)
  - Static CMOS
  - Complex Logic Gates
  - Pass Transistor Logic

- The designer has complete control over what is placed on silicon and governed only by cost and performance

- New logic design strategies have been proposed recently and others will likely emerge in the future

- The digital designer needs to be familiar with the benefits and limitations of varying logic styles to come up with a good solution for given system requirements
Basic Logic Circuits

With an improved Switch-Level Model of the Transistor
An important performance metric of logic gates is SPEED

According to the ideal switch-level model (the open/short view of the transistor), the output responds to the input immediately (infinite speed) → Too good to be true

Something is missing!
The ideal switch-level model of MOSFET was developed

Simple logic gates designed in CMOS Process were introduced

- Some have zero power dissipation
- Some have or appeared to have rail to rail logic voltage swings
- All appeared to be Infinitely fast
- Logic levels of some can not be predicted with the ideal switch-level model
- The ideal switch-level model is not sufficiently accurate to provide insight relating to some of these properties

MOSFET modeling strategy

- Hierarchical model structure will be developed
- Generally use simplest model that can be justified
MOSFET Modeling: The Ideal Switch-Level Model

◆ Advantages

➢ Simple, does not require understanding of semiconductor properties, does not depend upon process, adequate for understanding basic operation of many digital circuits

◆ Limitations

➢ Does not provide performance information (such as speed)
➢ Can not support design of the “resistor” used in Pass Transistor Logic
The n-Channel MOSFET: Ideal Switch Model

![Diagram of n-channel MOSFET]

\[G = 0\]  \hspace{2cm}  \[G = 1\]
The n-Channel MOSFET: Improved Switch Model

- A more realistic view ➔ When the transistor is on, the channel has a non-zero resistance
- The Bulk is typically connected to the lowest voltage in the circuit

For small $V_{GS}$

For large $V_{GS}$
The n-Channel MOSFET: Improved Switch Model

- Capacitance from gate to channel region is distributed, but lumped capacitance is much easier to work with.

For small $V_{GS}$

For large $V_{GS}$
The n-Channel MOSFET: Improved Switch Model

- Capacitance from gate to channel region is distributed, but lumped capacitance is much easier to work with

For small $V_{GS}$:

For large $V_{GS}$:
The n-Channel MOSFET: Improved Switch Model

◆ Assuming the bulk is connected to the source

Switch-level model including gate capacitance and drain resistance

Switch is closed for high $V_{GS}$ (“1”)
The n-Channel MOSFET: Improved Switch Model

Improved Switch-level model including gate capacitance and drain resistance

Switch is closed for high $V_G$ ("1")

Ideal Switch-level model
The p-Channel MOSFET: Improved Switch Model

Improved Switch-level model including gate capacitance and drain resistance

Switch is closed for low $V_G$ ("0")

Ideal Switch-level model

Improved Switch-level model including gate capacitance and drain resistance
The MOSFET: Improved Switch Model

- $C_{GS}$ and $R_{SW}$ depend on device size and process
- For minimum-sized devices in a 0.5μ process

\[ C_{GS} \approx 1.5fF \quad R_{SW} \approx \begin{cases} 2K\Omega & \text{n-channel} \\ 6K\Omega & \text{p-channel} \end{cases} \]

- Considerable emphasis will be placed upon device sizing to manage $C_{GS}$ and $R_{SW}$

Improved Switch-level model including gate capacitance and drain resistance

Switch is closed for high $V_G$ ("1")
The MOSFET: Improved Switch Model

◆ Making sense of 1.5fF → Is that big or small? Can it be neglected?

Area allocations shown to relative scale
The MOSFET: Improved Switch Model

- Not enough information at this point to determine whether this seemingly very small capacitance can be neglected or not
- Will answer this important question later

Area allocations shown to relative scale
Logic Circuits: Quantifying Speed

- How long does it take for the output of a digital gate to change in response to a change in the input → Delay

\[ t_{HL}, t_{LH} \]

A \rightarrow Y

\[ C_L \]
Example → Find $t_{HL}$ and $t_{LH}$ for a minimum size inverter with 1pF load in 0.5$\mu$m technology using the ideal switch-level models and the improved switch-level models.
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Logic Circuits: Quantifying Speed

- With ideal switch-level model

\[ t_{HL} = t_{LH} = 0 \]

- Charging or discharging a capacitance through a zero-resistance switch is immediate \( t_{HL} = t_{LH} = 0 \)
Logic Circuits: Quantifying Speed

- With improved switch-level model

- Charging or discharging a capacitance through a non-zero resistance switch takes some time → $t_{HL}$ and $t_{LH} \neq 0$
Logic Circuits: Quantifying Speed

- Determining $t_{HL} \rightarrow$ Assume $V_{DD}$ is 5V

5V is the initial condition on $C_L$
Determining $t_{HL} \rightarrow$ Assume $V_{DD}$ is 5V

Recognize as a first-order RC network

Recall: Step response of any first-order network with LHP pole can be written as

$$y(t) = F + (I - F)e^{-\frac{t}{\tau}}$$

where $F$ is the final value, $I$ is the initial value and $\tau$ is the time constant of the circuit

For the circuit above, $F=0$, $I=5$ and $\tau = R_{SWn} C_L$
Logic Circuits: Quantifying Speed

Determining $t_{HL}$ → Assume $V_{DD}$ is 5V

How is $t_{HL}$ defined?

$V_{OUT}(t) = F + (1 - F)e^{\frac{t}{\tau}}$

$V_{OUT}(t) = 5e^{\frac{t}{\tau}}$

$\tau = R_{SWn} C_L$
Logic Circuits: Quantifying Speed

- Determining $t_{HL}$: Defined to be the time taken for the output to drop to $I/e$
- This definition has proved useful at analytically predicting response time of circuits

\[
V_{OUT}(t) = F + (I - F) e^{-\frac{t}{\tau}}
\]

\[
\frac{I}{e} = F + (I - F) e^{-\frac{t_{HL}}{\tau}}
\]
Logic Circuits: Quantifying Speed

Determining $t_{HL}$

\[
\frac{1}{e} = F + (I - F)e^{-\frac{t_{HL}}{\tau}}
\]

\[
\frac{1}{e} = 0 + (1 - 0)e^{-\frac{t_{HL}}{\tau}}
\]

\[
\frac{1}{e} = e^{-\frac{t_{HL}}{\tau}}
\]

\[t_{HL} = \tau\]

\[t_{HL} = R_{SWn} C_L\]
Determining $t_{\text{LH}} \rightarrow$ Assume $V_{\text{DD}}$ is 5V

Upper switch closes at time $t=0$

$0V$ is the initial condition on $C_L$
Determining $t_{LH} \rightarrow$ Assume $V_{DD}$ is 5V

$y(t) = F + (1 - F)e^{-\frac{t}{\tau}}$

*For this circuit, $F=5$, $I=0$ and $\tau = R_{SWP}C_L$*
Logic Circuits: Quantifying Speed

- Determining $t_{LH}$ → Assume $V_{DD}$ is 5V

How is $t_{LH}$ defined?

$$V_{OUT}(t) = F + (1 - F)e^{\frac{-t}{\tau}}$$

$$V_{OUT}(t) = 5\left(1 - e^{\frac{-t}{\tau}}\right)$$

$$\tau = R_{SWP}C_L$$
Logic Circuits: Quantifying Speed

- Determining $t_{LH} \rightarrow$ Defined to be the time taken for the output to rise to $(F - F/e)$
- This definition has proved useful at analytically predicting response time of circuits

$V_{OUT}(t) = F + (I - F) e^{-\frac{t}{\tau}} \\ F \left( 1 - \frac{1}{e} \right) = F + (I - F) e^{-\frac{t_{LH}}{\tau}}$
Logic Circuits: Quantifying Speed

- **Determining \( t_{LH} \)**

\[
F \left(1 - \frac{1}{e}\right) = F + (1 - F) e^{-\frac{t_{LH}}{\tau}}
\]

\[
F \left(1 - \frac{1}{e}\right) = F + (F) e^{-\frac{t_{LH}}{\tau}}
\]

\[
1 - \frac{1}{e} = 1 + e^{-\frac{t_{LH}}{\tau}}
\]

\[
t_{LH} = \tau
\]

\[
t_{LH} = R_{SWp} C_L
\]
Logic Circuits: Quantifying Speed

Determining $t_{HL}$ and $t_{LH}$ for a minimum size inverter with a 1pF load in 0.5µ technology using the improved switch-level models

$$t_{HL} \approx R_{SWn} C_L = 2k \times 1pF = 2\text{ns}$$

$$t_{LH} \approx R_{SWp} C_L = 6k \times 1pF = 6\text{ns}$$
Logic Circuits: Quantifying Speed

- Determining $t_{HL}$ and $t_{LH}$ for a minimum size inverter with a 1pF load in 0.5µ technology using the improved switch-level models

$$t_{HL} \approx R_{SWn} C_L = 2k \times 1pF = 2\text{ns} \quad t_{LH} \approx R_{SWp} C_L = 6k \times 1pF = 6\text{ns}$$

- Note that $C_L$ alone is not enough to determine speed $\rightarrow R_{SW}$ is equally important

- Note that this circuit is quite fast

- Note that $t_{HL}$ is much shorter than $t_{LH}$

- Often $C_L$ will be even smaller and the circuit will be much faster
Logic Circuits: Quantifying Speed

Example \( \rightarrow \) Find \( t_{HL} \) and \( t_{LH} \) for a minimum size inverter driving another minimum size inverter in 0.5\( \mu \)m technology using the improved switch-level models.

\[
Y \quad C_L = ?
\]

For convenience, will reference both to ground.

\[
C_{GSp} + C_{GSn} \quad 3fF
\]
Example → Find $t_{HL}$ and $t_{LH}$ for a minimum size inverter driving another minimum size inverter in 0.5µ technology using the improved switch-level models

$t_{HL} \approx R_{SWn} C_L$

$= 2k \times 3fF = 6ps$

$t_{LH} \approx R_{SWp} C_L$

$= 6k \times 3fF = 18ps$
Logic Circuits: Quantifying Speed

- Determining $t_{\text{HL}}$ and $t_{\text{LH}}$ a minimum size inverter driving another minimum size inverter in 0.5µ technology using the improved switch-level models

$$t_{\text{HL}} \approx R_{\text{SWn}} C_L = 2k \times 3\text{fF} = 6\text{ps} \quad t_{\text{LH}} \approx R_{\text{SWp}} C_L = 6k \times 3\text{fF} = 18\text{ps}$$

- Note that the circuit is very fast, but $C_L$ can’t just be ignored

- Judging whether $C_L$ is small or big must take into account the desired speed and the resistance