EE330
Integrated Electronics

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Basic Logic Circuits

An Application to the MOS Transistor
Pass Transistor Logic

- Standard static logic as well as complex logic gates require more complexity in order to implement basic non-inverting logic functions.

\[ Y = A \cdot B \]

6 transistors and 2 logic levels
Consider the simple AND function

\[ Y = A \cdot B \]

Requires only 2 transistors rather than 6 for a standard CMOS gate (and a resistor)
Pass Transistor Logic

◆ Consider the simple AND function \( \rightarrow \) Even simpler pass transistor logic implementations are possible

\[
Y = A \cdot B
\]

◆ Requires only 1 transistor and a resistor
Pass Transistor Logic

- Consider the XOR function

\[ Y = A \oplus B \]

- Requires only 6 transistors and 1 resistor, with two levels of logic
Consider the XOR function → eliminating the inverters is possible

\[ Y = A \oplus B \]

Requires only 2 transistors and 1 resistor, with 1 level of logic
Pass Transistor Logic

- Pass transistor logic is actually commonly used
- It offers significant reductions in complexity for some functions (particularly non-inverting)

- But life can’t be so good → There is always a caveat
  - The resistor may require more area than several hundred or even several thousand transistors
  - Signal levels may not go to VDD or to 0V
  - Static power dissipation may not be zero
  - Signals may degrade unacceptably if multiple gates are cascaded

- The “resistor” is often implemented with a transistor to reduce area but signal swing and power dissipation problems still persist
Logic Design Styles: A Summary

Several different logic design styles are often used throughout a given design (3 considered thus far)
- Static CMOS
- Complex Logic Gates
- Pass Transistor Logic

The designer has complete control over what is placed on silicon and governed only by cost and performance.

New logic design strategies have been proposed recently and others will likely emerge in the future.

The digital designer needs to be familiar with the benefits and limitations of varying logic styles to come up with a good solution for given system requirements.
Basic Logic Circuits

With an improved Switch-Level Model of the Transistor
An important performance metric of logic gates is SPEED

According to the ideal switch-level model (the open/short view of the transistor), the output responds to the input immediately (infinite speed) → Too good to be true

Something is missing!
MOSFET Modeling

◆ The ideal switch-level model of MOSFET was developed
◆ Simple logic gates designed in CMOS Process were introduced
  ➢ Some have zero power dissipation
  ➢ Some have or appeared to have rail to rail logic voltage swings
  ➢ All appeared to be Infinitely fast
  ➢ Logic levels of some can not be predicted with the ideal switch-level model
  ➢ The ideal switch-level model is not sufficiently accurate to provide insight relating to some of these properties

◆ MOSFET modeling strategy
  ➢ Hierarchical model structure will be developed
  ➢ Generally use simplest model that can be justified
MOSFET Modeling: The Ideal Switch-Level Model

◆ Advantages
  ➢ Simple, does not require understanding of semiconductor properties, does not depend upon process, adequate for understanding basic operation of many digital circuits

◆ Limitations
  ➢ Does not provide performance information (such as speed)
  ➢ Can not support design of the “resistor” used in Pass Transistor Logic
The n-Channel MOSFET: Ideal Switch Model

\[ D = S = G = 0 \quad \text{and} \quad D = S = G = 1 \]
The n-Channel MOSFET: Improved Switch Model

- A more realistic view ➔ When the transistor is on, the channel has a non-zero resistance
- The Bulk is typically connected to the lowest voltage in the circuit

For small $V_{GS}$

For large $V_{GS}$
The n-Channel MOSFET: Improved Switch Model

Capacitance from gate to channel region is distributed, but lumped capacitance is much easier to work with

For small $V_{GS}$

For large $V_{GS}$
The n-Channel MOSFET: Improved Switch Model

- Assuming the bulk is connected to the source

Switch-level model including gate capacitance and drain resistance

Switch is closed for high $V_{GS}$ ("1")
The n-Channel MOSFET: Improved Switch Model

Improved Switch-level model including gate capacitance and drain resistance

Ideal Switch-level model

Switch is closed for high $V_G$ ("1")
The p-Channel MOSFET: Improved Switch Model

Improved Switch-level model including gate capacitance and drain resistance

Switch is closed for low $V_G$ ("0")

Ideal Switch-level model

Switch is closed for low $V_G$ ("0")
The MOSFET: Improved Switch Model

- $C_{GS}$ and $R_{SW}$ depend on device size and process
- For minimum-sized devices in a 0.5u process

$$C_{GS} \approx 1.5fF \quad R_{SW} \approx \begin{cases} 2K\Omega & \text{n-channel} \\ 6K\Omega & \text{p-channel} \end{cases}$$

- Considerable emphasis will be placed upon device sizing to manage $C_{GS}$ and $R_{SW}$

Improved Switch-level model including gate capacitance and drain resistance

Switch is closed for high $V_G$ ("1")
The MOSFET: Improved Switch Model

- Making sense of 1.5fF → Is that big or small? Can it be neglected?

Area allocations shown to relative scale
The MOSFET: Improved Switch Model

- Not enough information at this point to determine whether this seemingly very small capacitance can be neglected or not
- Will answer this important question later

Area allocations shown to relative scale
Logic Circuits: Quantifying Speed

- How long does it take for the output of a digital gate to change in response to a change in the input → Delay

![Diagram of a digital gate with delay times labeled as $t_{HL}$ and $t_{LH}$]
Example → Find $t_{HL}$ and $t_{LH}$ for a minimum size inverter with 1pF load in 0.5µ technology using the ideal switch-level models and the improved switch-level models.
Example → Find $t_{HL}$ and $t_{LH}$ for a minimum size inverter with 1pF load in 0.5µ technology using the ideal switch-level models and the improved switch-level models.
Logic Circuits: Quantifying Speed

- **With ideal switch-level model**

  ![Diagram of an ideal switch-level model with a capacitance of 1pF and variables t_{HL}=t_{LH}=0.]

- **Charging or discharging a capacitance through a zero-resistance switch is immediate → t_{HL}=t_{LH}=0**

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EE330, Spring 2014, Lecture # 7
Logic Circuits: Quantifying Speed

- With improved switch-level model

- Charging or discharging a capacitance through a non-zero resistance switch takes some time \( t_{HL} \) and \( t_{LH} \neq 0 \)
Logic Circuits: Quantifying Speed

◆ Determining $t_{HL} \rightarrow$ Assume $V_{DD}$ is 5V

Lower switch closes at time $t=0$

5V is the initial condition on $C_L$
Logic Circuits: Quantifying Speed

Determining $t_{HL} \rightarrow$ Assume $V_{DD}$ is 5V

Recall: Step response of any first-order network with LHP pole can be written as

$$y(t) = F + (I - F)e^{-\frac{t}{\tau}}$$

where $F$ is the final value, $I$ is the initial value and $\tau$ is the time constant of the circuit

For the circuit above, $F=0$, $I=5$ and $\tau = R_{Swn}C_L$
Determining $t_{HL} \rightarrow$ Assume $V_{DD}$ is 5V

$V_{OUT}(t) = F + (1 - F)e^{\frac{t}{\tau}}$

$V_{OUT}(t) = 5e^{\frac{t}{\tau}}$

$\tau = R_{SWn}C_L$

How is $t_{HL}$ defined?
Logic Circuits: Quantifying Speed

- Determining $t_{HL} \rightarrow$ Defined to be the time taken for the output to drop to $I/e$
- This definition has proved useful at analytically predicting response time of circuits

\[ V_{OUT}(t) = F + (I - F)e^{-\frac{t}{\tau}} \]

\[ \frac{I}{e} = F + (I - F)e^{-\frac{t_{HL}}{\tau}} \]

\[ I = 5V, \quad F = 0V \]

\[ \tau = R_{SWn} C_L \]
Determining $t_{HL}$ →

\[
\frac{1}{e} = F + (1 - F) e^{-\frac{t_{HL}}{\tau}}
\]

\[
\frac{1}{e} = 0 + (1 - 0) e^{-\frac{t_{HL}}{\tau}}
\]

\[
\frac{1}{e} = e^{-\frac{t_{HL}}{\tau}}
\]

\[t_{HL} = \tau\]

\[t_{HL} = R_{SWn} C_L\]
Logic Circuits: Quantifying Speed

◆ Determining $t_{LH} \rightarrow$ Assume $V_{DD}$ is 5V

Upper switch closes at time $t=0$

0V is the initial condition on $C_L$
Logic Circuits: Quantifying Speed

- Determining $t_{LH} \rightarrow$ Assume $V_{DD}$ is 5V

For this circuit, $F=5$, $I=0$ and $\tau = R_{SWp} C_L$

$$y(t) = F + (1 - F) e^{-\frac{t}{\tau}}$$
**Logic Circuits: Quantifying Speed**

- **Determining $t_{LH}$ → Assume $V_{DD}$ is 5V**

![Circuit Diagram]

$$V_{OUT}(t) = F + (1-F)e^{\frac{t}{\tau}}$$

$$\tau = R_{SWp}C_L$$

**How is $t_{LH}$ defined?**
Logic Circuits: Quantifying Speed

- Determining $t_{LH} \rightarrow$ Defined to be the time taken for the output to rise to $(F - F/e)$
- This definition has proved useful at analytically predicting response time of circuits

\[ V_{OUT}(t) = F + (I - F)e^{\frac{t}{\tau}} \]

\[ F \left(1 - \frac{1}{e}\right) = F + (I - F)e^{\frac{t_{LH}}{\tau}} \]
Logic Circuits: Quantifying Speed

◆ Determining $t_{LH}$

$$F \left( 1 - \frac{1}{e} \right) = F + (1 - F) e^{-\frac{t_{LH}}{\tau}}$$

$$F \left( 1 - \frac{1}{e} \right) = F + (F) e^{-\frac{t_{LH}}{\tau}}$$

$$1 - \frac{1}{e} = 1 + e^{-\frac{t_{LH}}{\tau}}$$

$$t_{LH} = \tau$$

$$t_{LH} = R_{SWp} C_L$$

$I = 0V, \quad F = 5V$
Determining $t_{HL}$ and $t_{LH}$ for a minimum size inverter with a 1pF load in 0.5µ technology using the improved switch-level models.

$$t_{HL} \approx R_{SWn} C_L$$

$$= 2k \times 1\text{pF} = 2\text{ns}$$

$$t_{LH} \approx R_{SWp} C_L$$

$$= 6k \times 1\text{pF} = 6\text{ns}$$
Logic Circuits: Quantifying Speed

Determining $t_{HL}$ and $t_{LH}$ for a minimum size inverter with a 1pF load in 0.5µ technology using the improved switch-level models

$$t_{HL} \approx R_{SWn} C_L = 2k \times 1pF = 2\text{ns} \quad t_{LH} \approx R_{SWp} C_L = 6k \times 1pF = 6\text{ns}$$

Note that $C_L$ alone is not enough to determine speed $\rightarrow R_{SW}$ is equally important

Note that this circuit is quite fast

Note that $t_{HL}$ is much shorter than $t_{LH}$

Often $C_L$ will be even smaller and the circuit will be much faster
Logic Circuits: Quantifying Speed

ハイパーリンク

Example → Find $t_{HL}$ and $t_{LH}$ for a minimum size inverter driving another minimum size inverter in 0.5µ technology using the improved switch-level models.

$A \rightarrow Y$  
$C_L = ?$

$Y \rightarrow \bar{Y}$  
$C_{GSn} \cong C_{GSp} \cong 1.5fF$

Loading effects same whether $C_{GSp}$ connected to $V_{DD}$ or GND

$Y \rightarrow C_{GSp} + C_{GSn}$  
For convenience, will reference both to ground

$Y \rightarrow 3fF$
Logic Circuits: Quantifying Speed

Example → Find $t_{HL}$ and $t_{LH}$ for a minimum size inverter driving another minimum size inverter in 0.5µ technology using the improved switch-level models.

\[
\begin{align*}
A & \rightarrow Y \\
A & \rightarrow Y \\
\text{3fF} & \\
\end{align*}
\]

\[
t_{HL} \approx R_{SWn} C_L = 2k \times 3fF = 6ps
\]

\[
t_{LH} \approx R_{SWp} C_L = 6k \times 3fF = 18ps
\]
Logic Circuits: Quantifying Speed

- Determining $t_{HL}$ and $t_{LH}$ a minimum size inverter driving another minimum size inverter in 0.5µ technology using the improved switch-level models

$$t_{HL} \approx R_{SWn} C_L = 2k \times 3fF = 6ps$$
$$t_{LH} \approx R_{SWp} C_L = 6k \times 3fF = 18ps$$

- Note that the circuit is very fast, but $C_L$ can’t just be ignored

- Judging whether $C_L$ is small or big must take into account the desired speed and the resistance