EE330
Integrated Electronics

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The Semiconductor Process

The Transistor, Reliability and Yield, Review of Basic Statistical Concepts, A Brief History
The Metal Oxide Semiconductor (MOS) Transistor

- A MOS transistor is formed through the overlap between two different materials → Poly-silicon (Poly) and n-type or p-type silicon (Active, and sometimes called Diffusion)
- The two materials are implemented on two vertically spaced levels → overlap does not mean intersection

![Diagram of MOS transistor]

- Poly
- Active

Bounding Region
The Metal Oxide Semiconductor (MOS) Transistor

- Although the area of the transistor is the bounding region, its functional portion (the Channel) is only the overlap → the rest is necessary to be able to connect to the transistor
- The geometric overlap is referred to as the Drawn Width (W) and Drawn Length (L) of the transistor

![Diagram of MOS Transistor with labeled dimensions W and L]
The Metal Oxide Semiconductor (MOS) Transistor

- Although the area of the transistor is the bounding region, its functional portion (the Channel) is only the overlap → the rest is necessary to be able to connect to the transistor.
- The actual source and drain is actually at the edge.

![Diagram of MOS Transistor with labels for Actual Source, Actual Drain, Gate, and Region of Interest (Channel) with dimensions W and L]
The Metal Oxide Semiconductor (MOS) Transistor

- The Effective width and length of the transistor are generally smaller than Drawn Width and Length.
The Feature Size

- The Feature Size is the minimum lateral size a certain feature can be reliably implemented in a given fabrication process
  - The minimum Width and Length of a transistor
  - The minimum metal interconnect width
  - The minimum spacing between metal interconnects
  - Etc…
The Feature Size

- Usually the Feature Size is the same for many features in a given technology
- Often specified in terms of pitch
- Pitch is approximately equal to twice minimum feature size
**Feature Size Evolution**

<table>
<thead>
<tr>
<th>Year</th>
<th>Feature Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mid 70's</td>
<td>25µ</td>
</tr>
<tr>
<td>2005</td>
<td>90nm</td>
</tr>
<tr>
<td>2010</td>
<td>20nm</td>
</tr>
<tr>
<td>2020</td>
<td>10nm</td>
</tr>
</tbody>
</table>

\[
1\mu = 10^3 \text{ nm} = 10^{-6} \text{ m} = 10^4 \text{ Å}
\]
Feature Size Evolution

- **Size of Atoms and Molecules in Semiconductor Processes**

  **Silicon:**
  - Average Atom Spacing: $2.7\,\text{Å}$
  - Lattice Constant: $5.4\,\text{Å}$

  **$\text{SiO}_2$:**
  - Average Atom Spacing: $3.5\,\text{Å}$
  - Breakdown Voltage: $5\text{ to } 10\text{MV/cm} = 5\text{ to } 10\text{mV/Å}$

- **Physical size of atoms and molecules place fundamental limit on conventional scaling approaches**

  **Air**: $20\text{KV/cm}$
Technology Nomenclature

- Depending on the number of transistors implemented in a given IC
  - SSI → Small Scale of Integration → 1-100
  - MSI → Medium Scale of Integration → 100-10^3
  - LSI → Large Scale of Integration → 10^3-10^5
  - VLSI → Very Large Scale of Integration → 10^5-10^6

- Any design in a process capable of incorporating a large number of devices is generally termed a VLSI design
The Die versus the Wafer

- The Die refers to the silicon area where a full design is implemented (this is what is inside the package of an IC)
- The Wafer is a large silicon disc that contains many copies of the same Die
- God bless the invention of copy/paste!

A Wafer is 6 inches to 12 inches in diameter with a flat edge very large number of die can be produced if die size is small.
Device and Die Cost

- Characterize the high-volume incremental costs of manufacturing integrated circuits

Example: Assume manufacturing cost of an 8” wafer in a 0.25µ process is $800

Determine the number of minimum-sized transistors that can be fabricated on this wafer and the cost per transistor. Neglect spacing and interconnect.

Solution:

\[ n_{\text{trans}} \approx \frac{A_{\text{wafer}}}{A_{\text{trans}}} = \frac{\pi (4\text{in})^2}{(0.25\mu)^2} = 5.2 \times 10^{11} \]

\[ C_{\text{trans}} = \frac{C_{\text{wafer}}}{n_{\text{trans}}} = \frac{\$800}{5.2 \times 10^{11}} = \$15.4 \times 10^{-9} \]

- Device count may be decreased by a factor of 10 or more if interconnect and spacing is included but even with this decrease, the cost per transistor is still very low!
Device and Die Cost

◆ From the previous example

\[ C_{\text{per unit area}} \approx \frac{2.5}{cm^2} \]

Example: If the die area of the 741 op amp is 1.8mm\(^2\) (including bonding pads), determine the cost of the silicon needed to fabricate this op amp

\[ C_{741} = \frac{2.5}{cm^2} \times (1.8mm^2) \approx 0.05 \]

Actual integrated op amp will be dramatically less if bonding pads are not needed.

◆ The smaller a circuit is \(\rightarrow\) the more copies you can fabricate on a single wafer \(\rightarrow\) the cheaper the circuit is even if the fabrication cost of the wafer stays the same.

◆ This is why we love scaling \(\rightarrow\) although fabrication cost may increase, reduction in the cost of the IC can decrease...
Reliability and Yield

The Feature Size is the minimum lateral size a certain feature can be reliably implemented in a given fabrication process → What does reliably actually mean?
Reliability and Yield

Upon fabricating a very large number of copies of a given feature or function, what is the probability that these copies will actually turn out to have the intended feature or function, or within an acceptable error from the intended feature or function?

If $P$ is the probability that a feature is “good”

$n$ is the number of features on an IC

$Y$ is the yield (probability that all features are simultaneously good)

$$Y = P \times P \times P \ldots \ldots = P^n$$

$$P = e^{\frac{\log_e Y}{n}}$$
Reliability and Yield

◆ How reliable must a given feature be?
◆ Let’s say the number of features n=5E3
◆ Let’s say we would like our yield to be Y=0.9

\[ P = e^{ \frac{\log_e Y}{n} } = e^{ \frac{\log_e 0.9}{5E3} } = 0.9999979 \]

◆ Is n=5E3 realistic? → Not really → n=5E9 is more like it!

\[ P = e^{ \frac{\log_e Y}{n} } = e^{ \frac{\log_e 0.9}{5E9} } = 0.999999999979 \]

◆ Extremely high reliability must be achieved per feature to obtain acceptable overall yields
◆ Yield dramatically affect Die and Device Cost
Yield Issues: Hard Faults

- Dust particles and other undesirable processes cause defects → These defects in manufacturing cause yield loss
Yield Issues: Hard Faults

- Defects in processing cause yield loss
- The probability of a defect causing a circuit failure increases with die area
- The circuit failures associated with these defects are termed **Hard Faults**
- This is the major factor limiting the size of die in integrated circuits
- Several different models have been proposed to model the hard faults
Yield Issues: Hard Fault Models

\[ Y_H = e^{-Ad} \]

- \( Y_H \) is the probability that the die does not have a hard fault.
- \( A \) is the die area.
- \( d \) is the defect density (typically \( 1\text{cm}^{-2} < d < 2\text{cm}^{-2} \)).

- **Industry often closely guards the value of \( d \) for their process.**
- **Other models, which may be better, have the same general functional form.**