Due Monday January 27 at the beginning of the lecture. You MUST clearly indicate your name and SECTION on the first page of your HW. Submissions that do not include the section WILL NOT be graded.

On this and subsequent HW assignments there will be problems that require a Verilog or VHDL solution. It will be assumed that students either have a background in Verilog or VHDL or that they will study what is needed to develop this background. There are numerous sources for material on Hardware Description Languages available on line. The text for the course also has a short discussion on HDL in Sec. 1.8 and a more extensive discussion in Appendix A. Please consult with your lab TA ahead of time if you need help locating Verilog or VHDL learning material.

Problem 1&2 (10 points each):
Please solve problems 1.1 & 1.5 of Weste and Harris (WH)

Problem 3 (10 points):
Assume a 12” wafer costs $1800. If the defect density on this wafer is 1.4/cm², determine the cost per good die if the die is square with a side dimension of 4mm.

Problem 4 (10 points):
If an amplifier has a specified offset voltage of 3mV (that is, |V_{OS}|<3mV), determine the soft yield if the standard deviation of the offset voltage is 2mV and the mean is 0V. Assume the distribution of the offset voltage is Gaussian.

Problem 5 (15 points):
Assume the offset voltage of an operational amplifier is a random variable and that the input offset voltage has a Gaussian distribution with a mean of 0V and a standard deviation of

\[ \sigma = \frac{A_{VT0}}{\sqrt{A}} \]

(he units are mV times a micrometer). Determine the area of the two input transistors if the input offset voltage is to be at most 2.5mV if a soft yield of 95% is required.

Problem 6 (15 points):
Assume a particular function in a 120nm process being used today requires a die area of 0.5cm² and is fabricated on 300mm wafers that cost $2000. The ITRS predicts that in 2012 the high-end processes will have 14nm feature sizes on 450mm wafers. If the 450mm wafers cost $3500 each, what will be the approximate cost per good die of the same function if fabricated in the new high-end process of 2012? When solving this problem, assume the circuit schematic does not change and neglect the bonding pad areas. Assume the defect density in both processes is the same and is 0.75/cm².
Problem 7 (10 points):
Design a Verilog system with inputs A, B, and C, and output F that implements the following function. Demonstrate the proper functioning of your circuit with full simulation. Do not simplify the equation.

\[ F = AB\bar{C} + A\bar{B}\bar{C} + \bar{A}BC \]

Problem 9 (20 points):
MTV is looking to streamline its production of *Jersey Shore* and has hired you to build a scene sorter. The sorter will have three inputs which MTV feels are crucial to the success of the show:

- Fist pumping (Input FIST)
- GTL (Input GTL)
- Snooki (Input SNOOKI)

The inputs will be Boolean high if the scene contains one of the inputs and low if it does not. It also has three outputs deciding where the scene will be shown:

- Both the episode and the previews (Output PREVIEW)
- Just the episode (Output EPISODE)
- Not used (Output GARBAGE)

If the scene contains two of the three inputs it will be used in the episode. If it contains all three, it will also be used in the preview. If it contains one or less it is not up to MTV's high journalistic standards and will not be used. Boolean high output will represent use in the show. Only one output should be high for a given scene. Design a scene sorter in Verilog with these three inputs and outputs. Demonstrate its correct function with proper simulation.